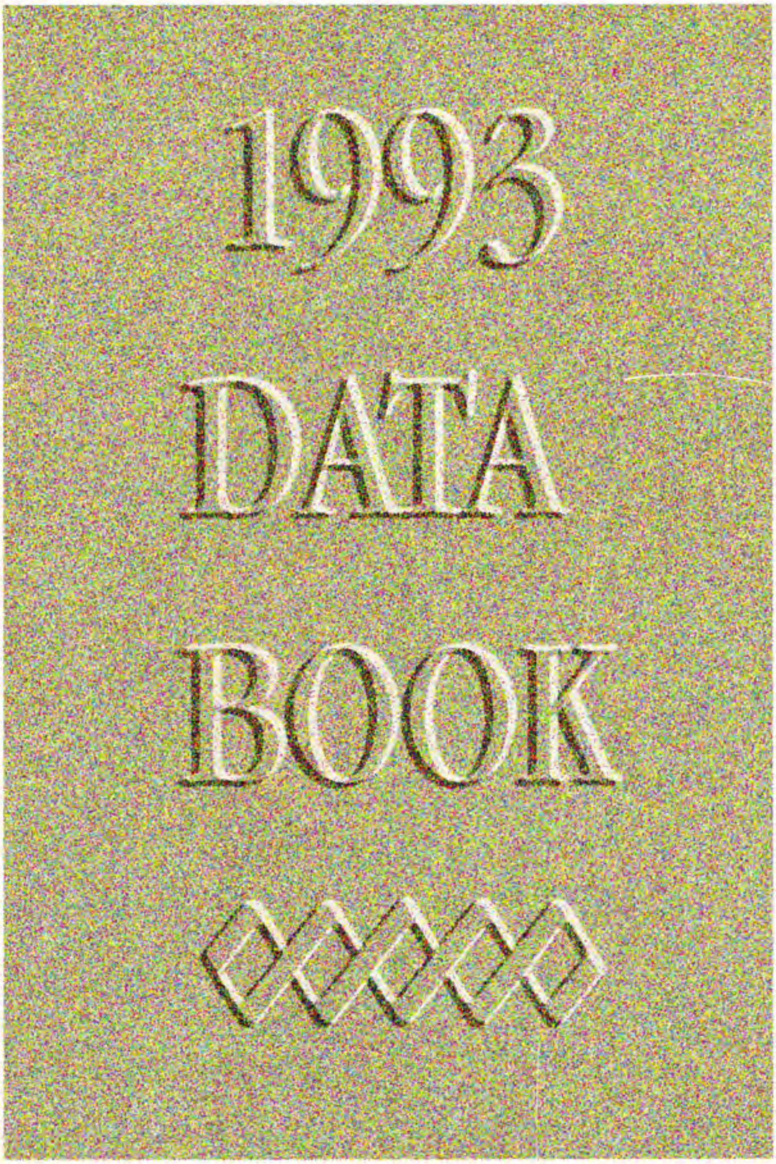

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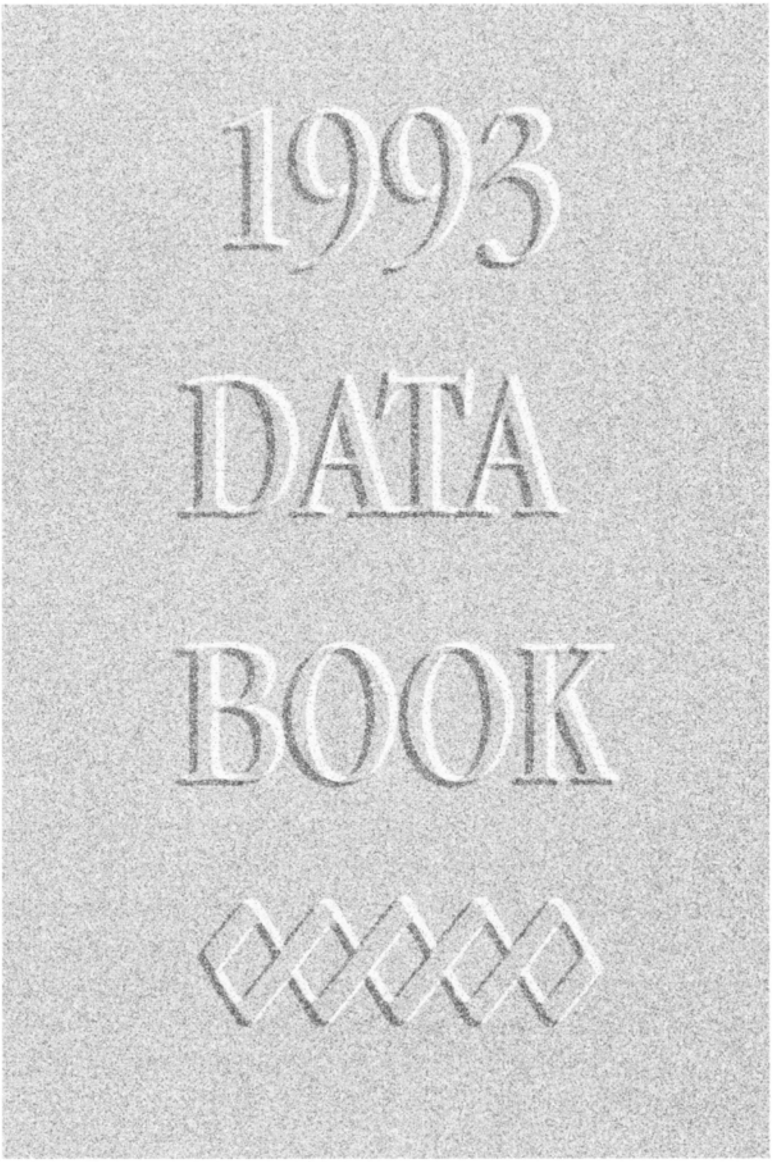

1993
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Introduction

Astec Semiconductor (ASD) was conceived in 1983 under a charter to design and manufacture high quality power conversion integrated circuits for the Astec family of power supply manufacturers.

Extending from this charter, we have become power supply specialists, developing semiconductor products optimized for the specific needs of the ever-changing power conversion market. Our products contain many unique features because we create products from a power supply designer's point of view. ASD takes pride in maintaining high specification standards, tight electrical parameters, practical operating temperatures, and long-term reliability.

ASD is completely dedicated to delivering products of the highest quality and performance for your power conversion applications.

Wayne E. Luty

Wayne E. Luty
Vice President, General Manager
Astec Semiconductor Division

Introduction

在１９８３年，ＡＳＤ（Ａｓｔｅｃ Ｓｅｍｉｃｏｎｄｕｃｔｏｒ Ｄｉｖｉｓｉｏｎ）受托爲Ａｓｔｅｃ雅達電子有限公司設計和生産高質量的電源變換集成電路．

隨着這種委托的發展，我們已經成爲開發優良半導體電源産品和滿足交換型電源供應器市場特殊需求的專家．　我們的産品據有許多獨特的性能，其原因在于，我們是以電源供應器設計者的觀點來創新我們的産品．　ＡＳＤ以保持高標准計術規範，嚴格的技術参數，和切合實際的運行温度和長期的可靠性而自豪．

ＡＳＤ完全獻身于提供高質量和高性能的産品，以滿足您電源供應器的需求．

Wayne E. Luty

韋恩．路蒂

副總裁，　總經理
雅達電子半導體（ＡＳＤ）

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General Information

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General Ordering Information

Order Entry

Products contained within this data book can be ordered from:

Astec Semiconductor
255 Sinclair Frontage Road
Milpitas, California 95035 USA
Phone: 408-263-8300
Facsimile: 408-263-8340

Ordering Information

Minimum engineering order: 50 pieces (product samples available upon request)

Minimum production order: 500 pieces

Each item ordered must appear exactly as listed in the data sheet

F.O.B.: Milpitas, California

Part Number Information

XX XXXX -XX

-XX — Package Style

XXXX — Generic or Product Part Number

XX — Designator

UC, TL, LM, and LT are industry standard second source devices
AS are proprietary or improved devices

Package Suffix Explanation

Letter Designation	Description
N	8, 14, 16, 18, and 20 Lead Plastic DIP
D	8, 14, and 16 Lead Plastic Narrow Body SOIC
DW	16, 18, and 20 Lead Plastic Wide Body SOIC
LP	TO-92 Plastic (3 Lead)
HP	TO-237 Plastic (3 Lead, TO-92 with Top Heat Spreader)
VS	SOT-23 Plastic (3 Lead)
S	SOT-89 Plastic (3 Lead with Heat Spreader)
G	SOT-223 Plastic (3 Lead with Heat Spreader)

Package Marking Explanation

Package marking provides a consistent way of identifying product types and managing lot traceability. All Astec products, with the exception of the SOT-23 and SOT-89 packages, are marked with product type, lot number, date code, and country of origin. Each assembly lot in the SOT-23 and SOT-89 packages, receives a unique alpha-numeric code which is recorded in a data base for cross reference to lot number, date code, and country of origin. A complete marking format table is shown below.

8, 14, 16, 18, and 20 Lead Plastic DIP:

Top- Astec Logo
Product Name
Lot Identificaton Code
Bottom - Lot Identification Code
Country of Origin
Date Code

8, 14, and 16 Lead Plastic Narrow Body SOIC:

Top- Product Name
Lot Identificaton Code
Bottom - Date Code
Country of Origin

16, 18, and 20 Lead Plastic Wide Body SOIC:

Top- Astec Logo
Product Name
Lot Identificaton Code
Bottom - Lot Identification Code
Country of Origin
Date Code

TO-92/237 Plastic (3 Lead):

Face- Astec Logo
Product Name
Lot Identificaton Code
Country of Origin
Date Code

SOT-23 Plastic (3 Lead):

Top- Log Book Code

SOT-89 Plastic (3 Lead with Heat Spreader):

Top- Product Name
Log Book Code

SOT-223 Plastic (3 Lead with Heat Spreader):

Top- Product Name
Lot Identificaton Code
Bottom - Date Code
Country of Origin

Alternate Source and Product Cross-Reference

P/N	ASD P/N
Cherry Semiconductor	
CS384xA	UC384x
CS384x	UC384x
Hitachi	
HA17431	A431
HA17384	UC3842
HA17345	UC3843
Linear Technology	
LM385-1.2	AS1004-1.2
LM385-2.5	AS1004-2.5
LT1004-1.2	AS1004-1.2
LT1004-2.5	AS1004-2.5
LT1431CZ	AS1431*
LT1242	UC3842*
LT1243	UC3843*
LT1244	UC3844*
LT1245	UC3845*
Motorola Semiconductor	
TL431	A431
TL431a	A431
UC384x	UC384x
UC384xA	UC384x
National Semiconductor	
LM431A	A431
LM385-1.2	AS1004-1.2
LM385-2.5	AS1004-2.5
Samsung Semiconductor	
SKA431	A431
KA384x	UC384x
Texas Instruments	
TL431	A431
TL431A	A431
TL1431	AS1431
LM385-1.2	AS1004-1.2
LM385-2.5	AS1004-2.5
LT1004-1.2	AS1004-1.2
LT1004-2.5	AS1004-2.5
UC384x	UC384x
Unitrode	
UC384x	UC384x
UC384xA	UC384x*

* Similar Device: Please consult data sheet to determinate the suitability of replacement for specific applications

Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Proposed Information	In Design	This data sheet contains the design specifications for product development. These specifications are subject to change. Further information will be published upon product release.
Preliminary	First Production	This data sheet contains preliminary data. Supplementary data will be published at a later date. Astec Semiconductor reserves the right to make changes at any time without notice in order to improve design and supply the best product possible.
No Identification Noted	Full Production	This data sheet contains final specifications and complete typical curves. Astec Semiconductor reserves the right to make changes at any time without notice in order to improve design and supply the best product possible.

Data Sheets

Notes

ASTEC

AS431

Precision Adjustable Shunt Reference

Features

- Temperature-compensated: 30 ppm/°C
- Trimmed 0.5% bandgap reference
- Internal amplifier with 150 mA capability
- Nominal temperature range extended to 105° C
- Low frequency dynamic output impedance: < 150 mΩ
- Low output noise
- Robust ESD protection

Description

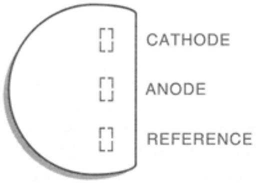
The AS431 is a three-terminal adjustable shunt regulator providing a highly accurate 0.5% bandgap reference. The adjustable shunt regulator is ideal for a wide variety of linear applications that can be implemented using external components to obtain adjustable currents and voltages.

In the standard shunt configuration, the combination of low temperature coefficient (T.C.), sharp turn-on characteristics, low output impedance and programmable output voltage make this precision reference a perfect zener diode replacement .

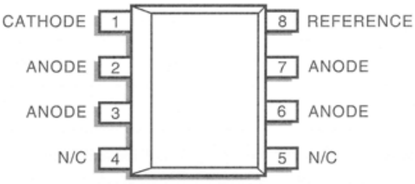
The A431 regulator is a low-cost solution where a bandgap reference tolerance is not critical. The A431 has a 1% bandgap reference and can be used as a direct replacement for the standard TL431.

Pin Configuration — Top view

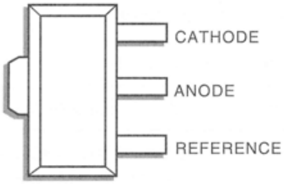
TO-92 (LP)



SOIC (D)



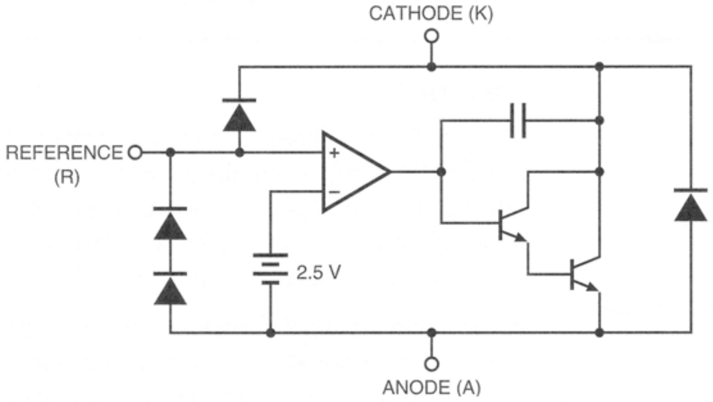
SOT-89 (S)



Ordering Information

Description	Temperature Range	Order Codes	
		0.5%	1.0%
TO-92	0 to 105° C	AS431LP	A431LP
8-Pin Plastic SOIC	0 to 105° C	AS431D	A431D
SOT-89	0 to 105° C	AS431S	A431S

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Cathode-Anode Reverse Breakdown	V_{KA}	37	V
Anode-Cathode Forward Current	I_{AK}	1	A
Operating Cathode Current	I_{KA}	250	mA
Reference Input Current	I_{REF}	10	mA
Continuous Power at 25° C	P_D		
TO-92		775	mW
8L SOIC		750	mW
SOT-89		1000	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	– 65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Cathode Voltage	V_{KA}	V_{REF} to 20	V
Cathode Current	I_K	10	mA

Typical Thermal Resistances

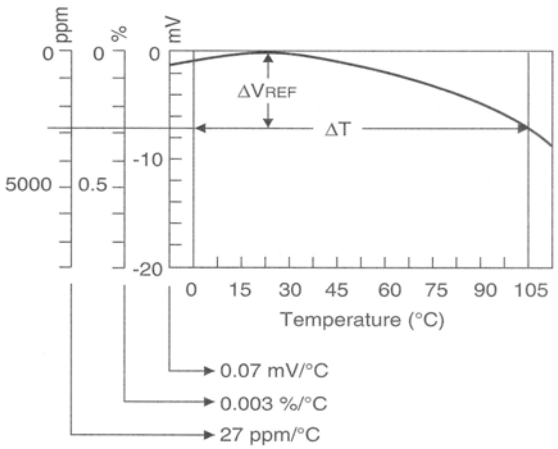
Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160° C/W	80° C/W	6.3 mW/°C
SOIC	175° C/W	45° C/W	5.7 mW/°C
SOT-89	110° C/W	8° C/W	9.1 mW/°C

Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{KA} = V_{REF}$ and $I_K = 10$ mA unless otherwise stated.

Parameter	Symbol	Test Condition	AS431 (0.5%)			A431 (1.0%)			Unit	Test Circuit
			Min	Typ	Max	Min	Typ	Max		
Reference Voltage	V_{REF}	$T_A = 25°$ C	2.490	2.503	2.515	2.470	2.495	2.520	V	1
		Over temp.	2.469	2.503	2.536	2.449	2.495	2.541	V	1
ΔV_{REF} with Temp*	TC			0.07	0.20		0.07	0.20	mV/ ° C	1
Ratio of Change in V_{REF} to Cathode Voltage	$\frac{\Delta V_{REF}}{\Delta V_K}$	V_{REF} to 10 V	− 2.7	− 1.01	− 2.7	− 1.0	1		mV/V	2
		10V to 36 V	− 2	− 0.4	0.3	− 2	− 0.4	0.3		
Reference Input Current	I_{REF}			0.7	4		0.7	4	µA	2
I_{REF} Temp Deviation	ΔI_{REF}	Over temp.		0.4	1.2		0.4	1.2	µA	2
Min I_K for Regulation	$I_{K(min)}$			0.4	1		0.4	1	mA	1
Off State Leakage	$I_{K(off)}$	$V_{REF} = 0$ V, $V_{KA} = 36$ V		0.04	250		0.04	250	nA	3
Dynamic Output Impedance	Z_{KA}	$f \leq 1$ kHz $I_K = 1$ to 50 mA		0.15	0.5		0.15	0.5	Ω	1

*Calculating Average Temperature Coefficient (TC)



- TC in mV/°C = $\dfrac{\Delta V_{REF}}{\Delta T_A}$

- TC in %/°C = $\dfrac{\left(\dfrac{\Delta V_{REF}}{V_{REF} \text{ at } 25°C}\right) \times 100}{\Delta T_A}$

- TC in ppm/°C = $\dfrac{\left(\dfrac{\Delta V_{REF}}{V_{REF} \text{ at } 25°C}\right) \times 10^6}{\Delta T_A}$

Test Circuits

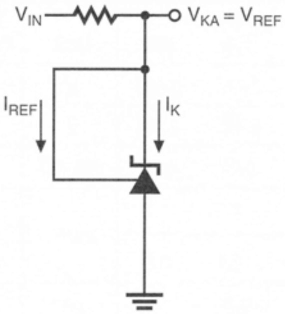


Figure 1a. Test Circuit 1

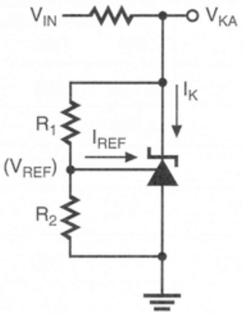


Figure 1b. Test Circuit 2

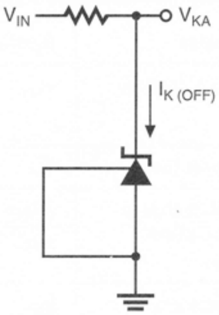


Figure 1c. Test Circuit 3

Typical Performance Curves

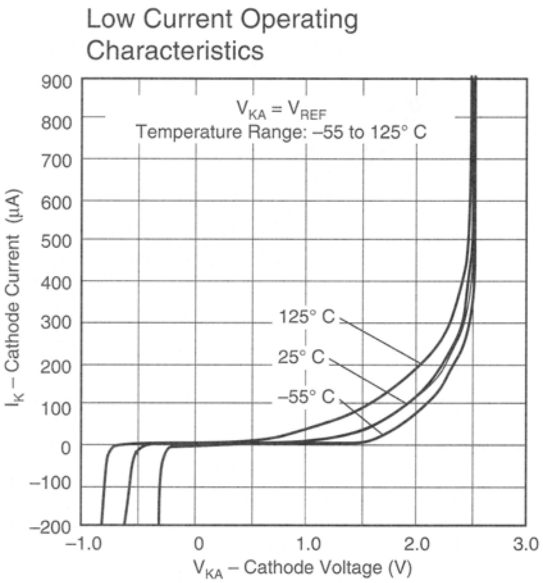


Figure 2

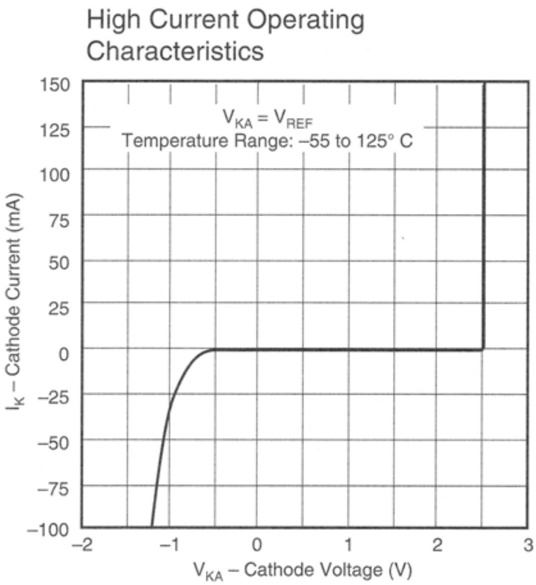


Figure 3

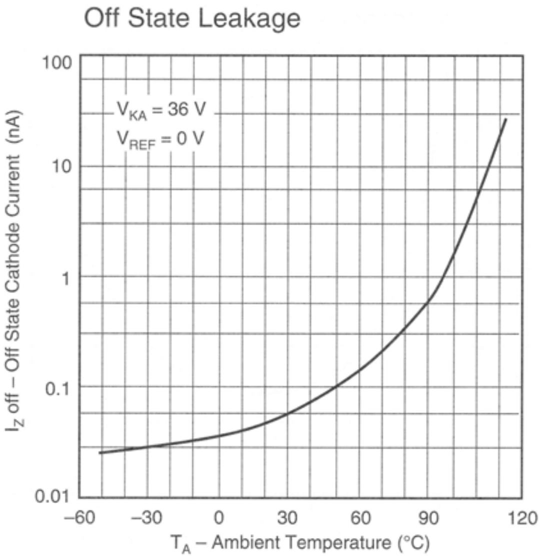


Figure 4

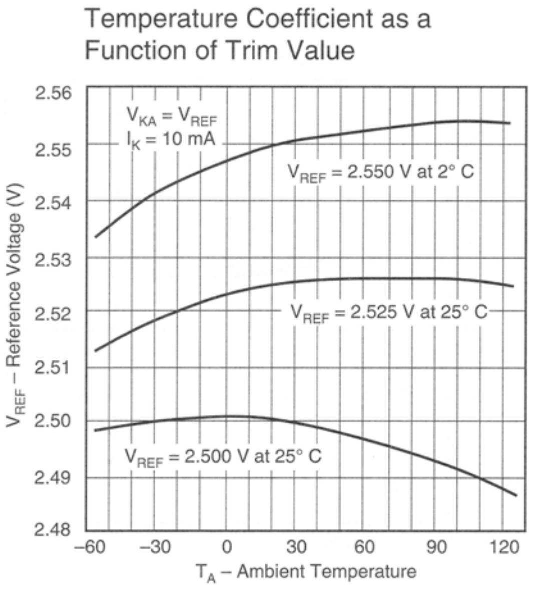
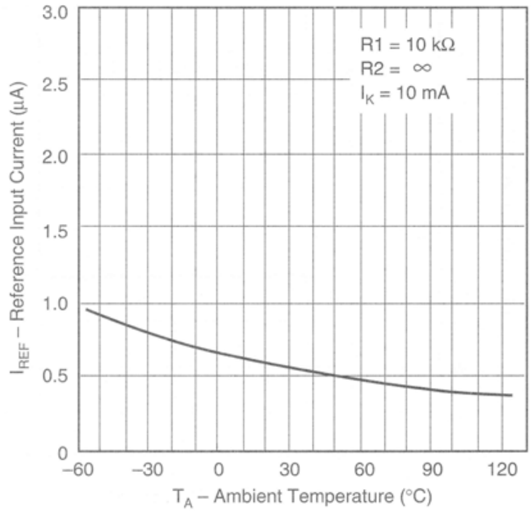


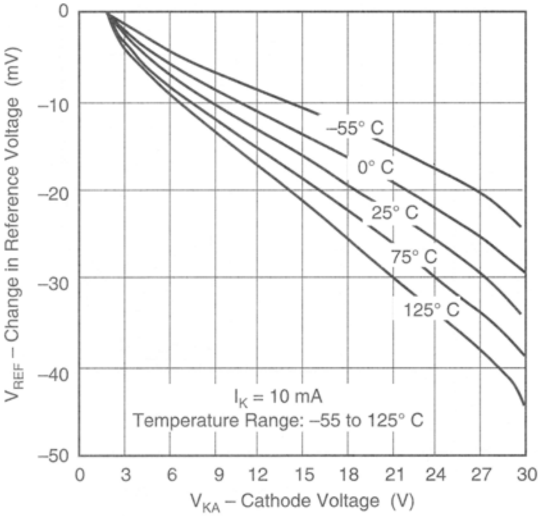
Figure 5

Typical Performance Curves



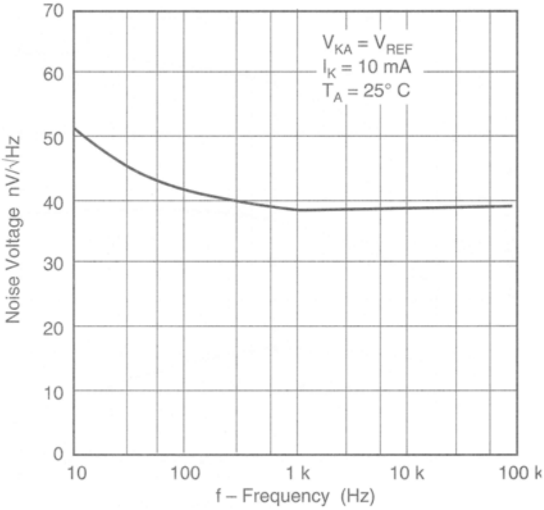
Reference Input Current

Figure 6



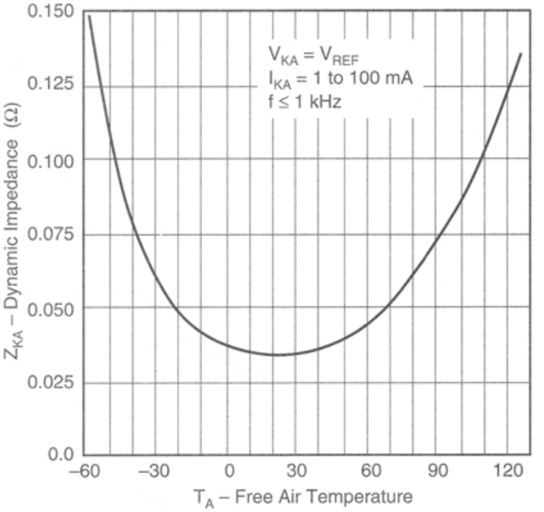
Reference Voltage Line Regulation

Figure 7



Noise Voltage

Figure 8



Low Frequency Dynamic Output Impedance

Figure 9

Typical Performance Curves

Dynamic Output Impedance

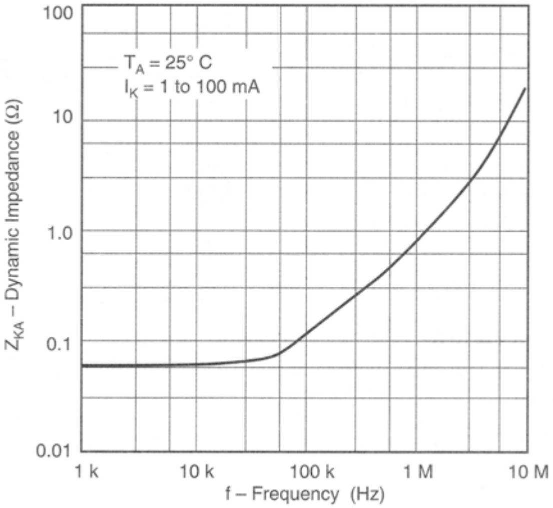
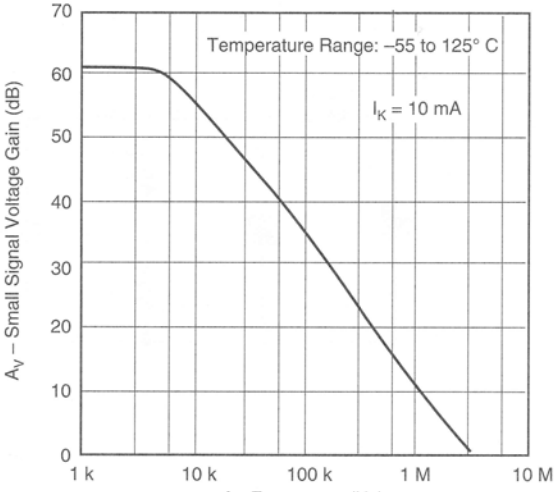


Figure 10

Small Signal Voltage Gain vs. Frequency



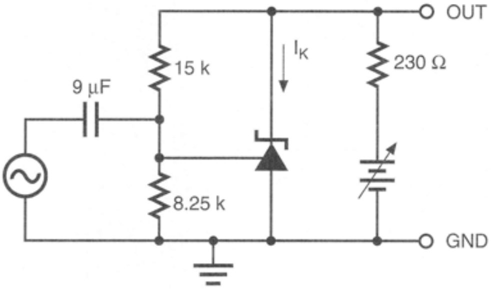
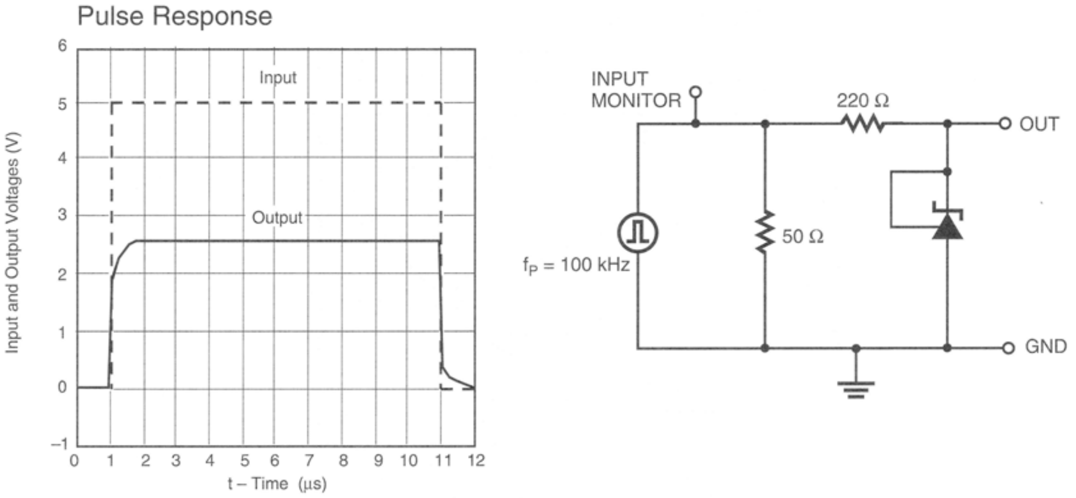


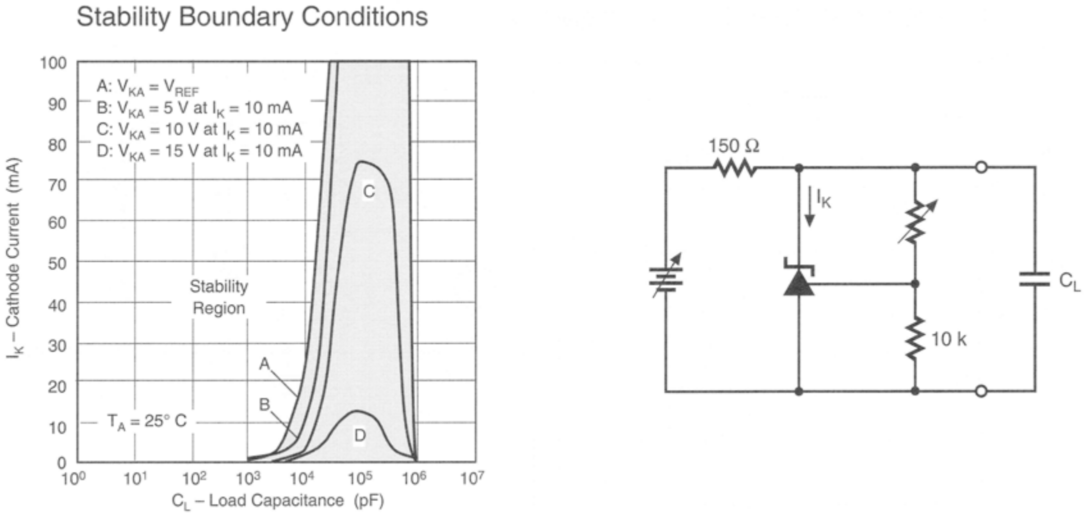
Figure 11

Typical Performance Curves



Pulse Response

Figure 12



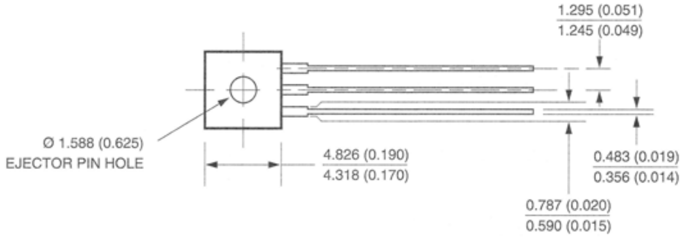
Stability Boundary Conditions

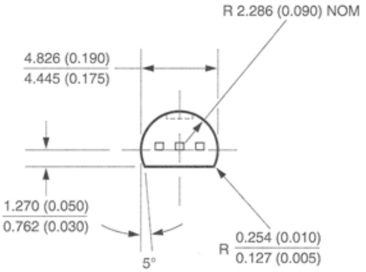
Figure 13

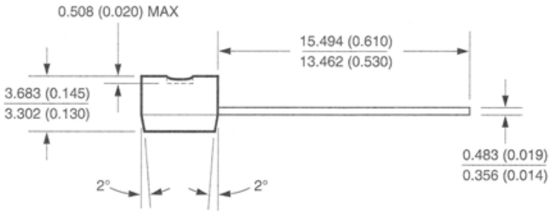
Package Dimensions

All Dimensions in mm (Inches)

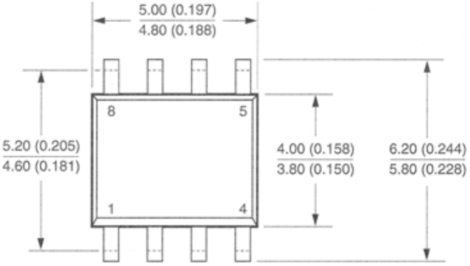
TO-92 Plastic (LP)

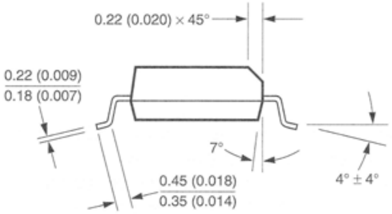


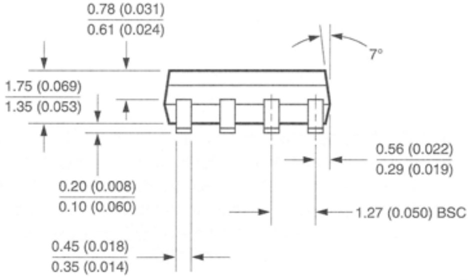




8-Pin Plastic SOIC (D)



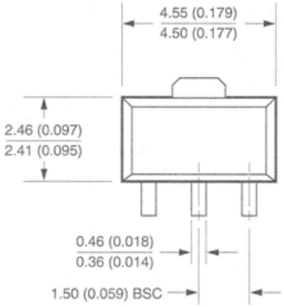


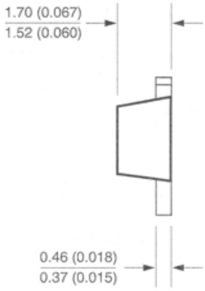


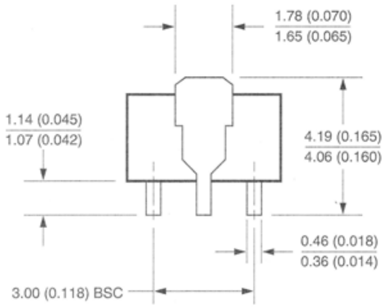
Package Dimensions

All Dimensions in mm (Inches)

SOT-89 (S)







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ASTEC SEMICONDUCTOR

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ASTEC

AS1431

Precision Adjustable Shunt Reference

Features

- Temperature-compensated: 30 ppm/°C
- Trimmed 0.4% bandgap reference
- Internal amplifier with 150 mA capability
- Temperature range: Extended to -55 to125° C
- Low frequency dynamic output impedance: < 150 mΩ
- Low output noise
- Robust ESD protection

Description

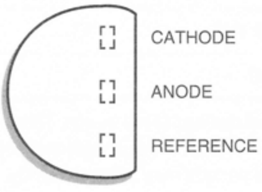
The AS1431 is a three-terminal adjustable shunt regulator providing a highly accurate 0.4% bandgap reference. The adjustable shunt regulator is ideal for a wide variety of linear applications that can be implemented using external components to obtain adjustable currents and voltages.

In the standard shunt configuration, the combination of low temperature coefficient (T.C.), sharp turn-on characteristics, low output impedance and programmable output voltage make this precision reference a perfect zener diode replacement .

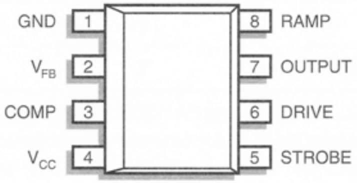
The AS1431 is characterized to operate over the full automotive temperature range of -55 to 125° C and is now available in the SOT-89 package.

Pin Configuration — Top view

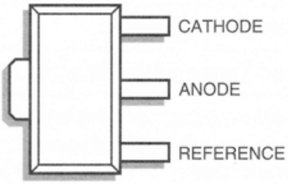
TO-92 (LP)



SOIC (D)



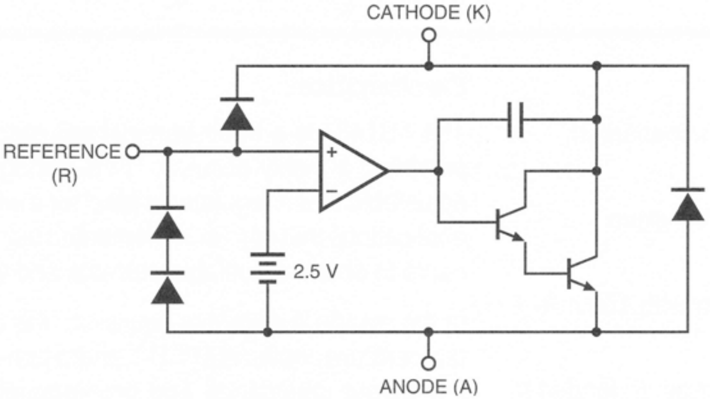
SOT-89 (S)



Ordering Information

Description	Temperature Range	Order Codes
TO-92	-55 to 125° C	AS1431LP
8-Pin Plastic SOIC	-55 to 125° C	AS1431D
SOT-89	-55 to 125° C	AS1431S

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Cathode-Anode Reverse Breakdown	V_{KA}	37	V
Anode-Cathode Forward Current	I_{AK}	1	A
Operating Cathode Current	I_{KA}	250	mA
Reference Input Current	I_{REF}	10	mA
Continuous Power Dissipation at 25° C	P_D		
TO-92		775	mW
8L SOIC		750	mW
SOT-89		1000	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	– 65 to 150	°C
Lead Temperature Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Cathode Voltage	V_{KA}	V_{REF} to 20	V
Cathode Current	I_K	10	mA

Typical Thermal Resistances

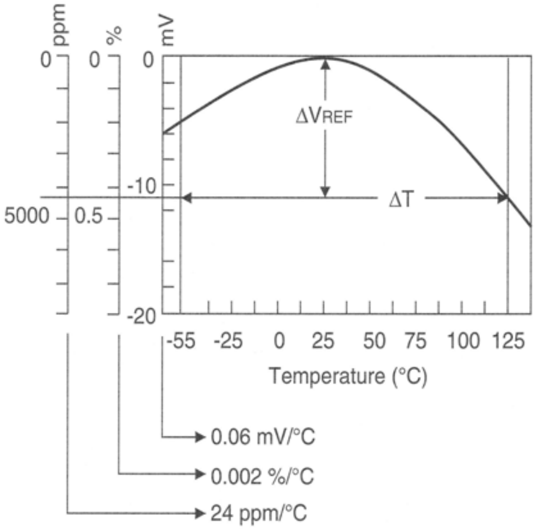
Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160° C/W	80° C/W	6.3 mW/°C
SOIC	175° C/W	45° C/W	5.7 mW/°C
SOT-89	110° C/W	8° C/W	9.1 mW/°C

Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (-55 to 125° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{KA} = V_{REF}$ and $I_K = 10$ mA unless otherwise stated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	Circuit
Reference Voltage	V_{REF}	$T_A = 25°$ C	2.490	2.500	2.510	V	1
		Over temp.	2.400	2.500	2.530	V	1
ΔV_{REF} with Temp*	TC			0.06	0.17	mV/ ° C	1
Ratio of Change in V_{REF} to Cathode Voltage	$\frac{\Delta V_{REF}}{\Delta V_K}$	V_{REF} to 10 V	− 2.7	− 1.01	− 2.7	mV/V	2
		10V to 36 V	− 2	− 0.4	0.3		
Reference Input Current	I_{REF}			0.7	4	µA	2
I_{REF} Temp Deviation	ΔI_{REF}	Over temp.		0.4	1.2	µA	2
Min I_K for Regulation	$I_{K(min)}$			0.4	1	mA	1
Off State Leakage	$I_{K(off)}$	$V_{REF} = 0$ V, $V_{KA} = 36$ V		0.04	500	nA	3
Dynamic Output Impedance	Z_{KA}	f ≤ 1 kHz $I_K = 1$ to 50 mA		0.15	0.5	Ω	1

*Calculating Average Temperature Coefficient (TC)



- TC in mV/°C = $\frac{\Delta V_{REF}}{\Delta T_A}$

- TC in %/°C = $\frac{\left(\frac{\Delta V_{REF}}{V_{REF}\text{ at }25°C}\right) \times 100}{\Delta T_A}$

- TC in ppm/°C = $\frac{\left(\frac{\Delta V_{REF}}{V_{REF}\text{ at }25°C}\right) \times 10^6}{\Delta T_A}$

Test Circuits

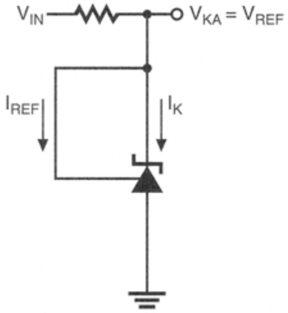


Figure 1a. Test Circuit 1

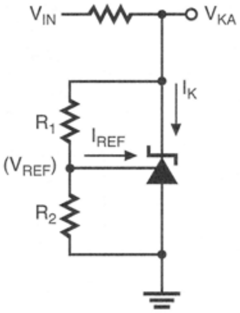


Figure 1b. Test Circuit 2

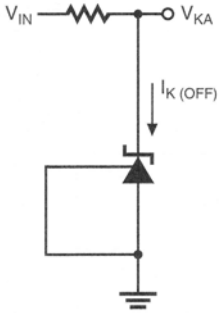


Figure 1c. Test Circuit 3

Typical Performance Curves

Low Current Operating Characteristics

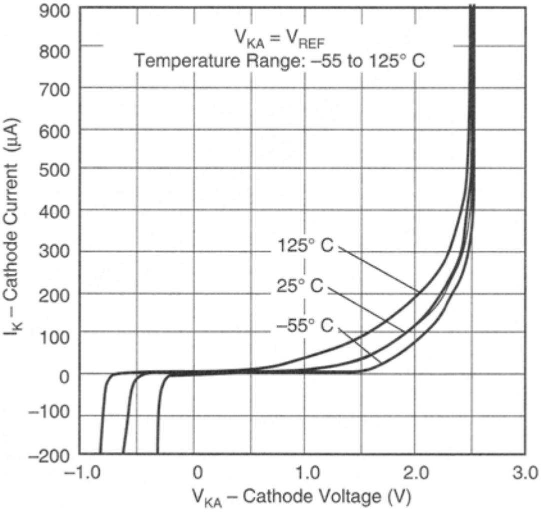


Figure 2

High Current Operating Characteristics

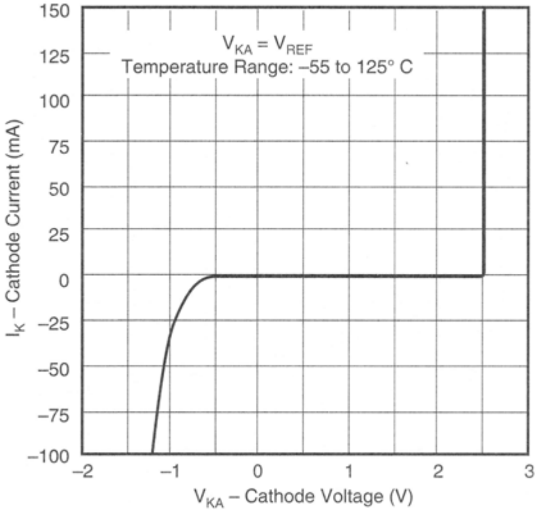


Figure 3

Off State Leakage

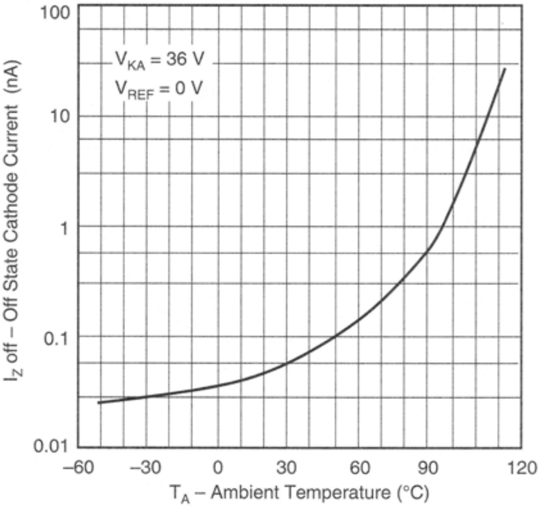


Figure 4

Reference Voltage vs Ambient Temperature

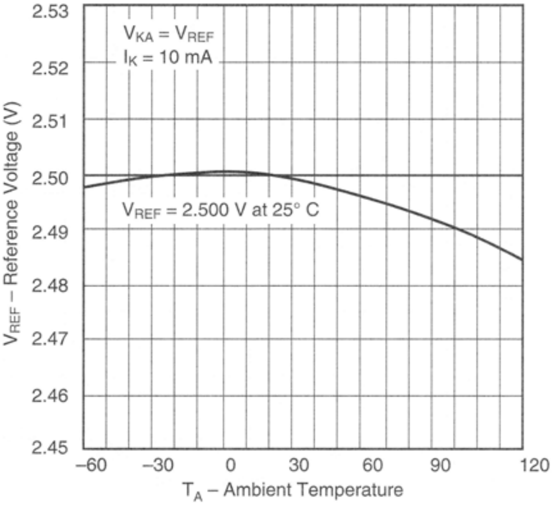
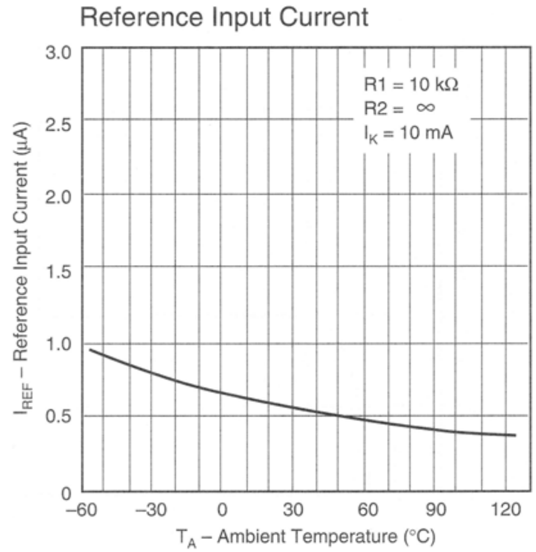


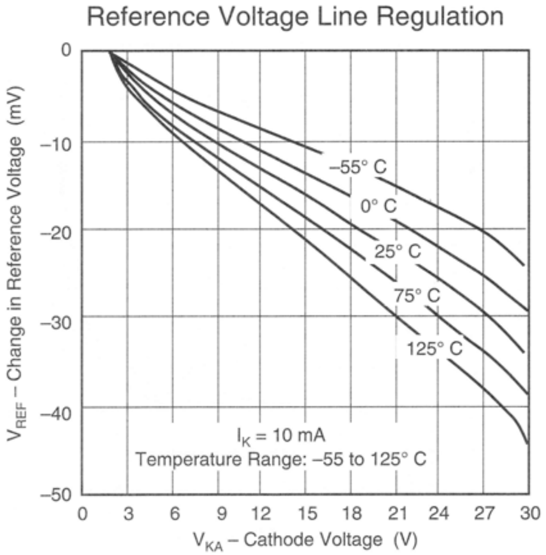
Figure 5

Typical Performance Curves



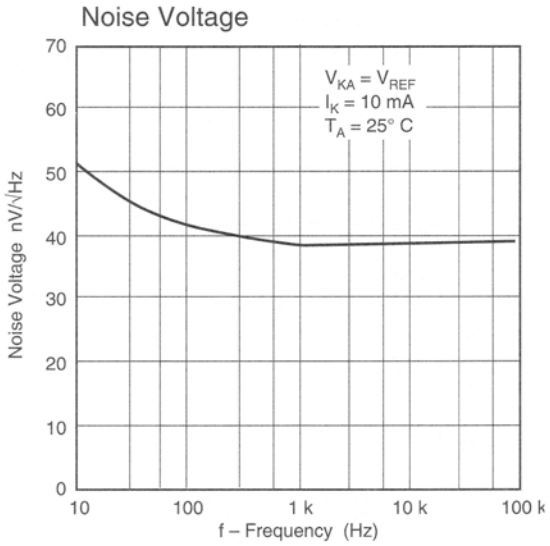
Reference Input Current

Figure 6



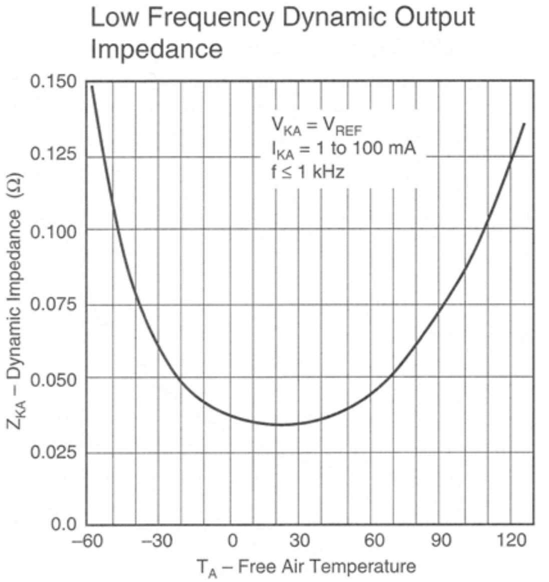
Reference Voltage Line Regulation

Figure 7



Noise Voltage

Figure 8



Low Frequency Dynamic Output Impedance

Figure 9

Typical Performance Curves

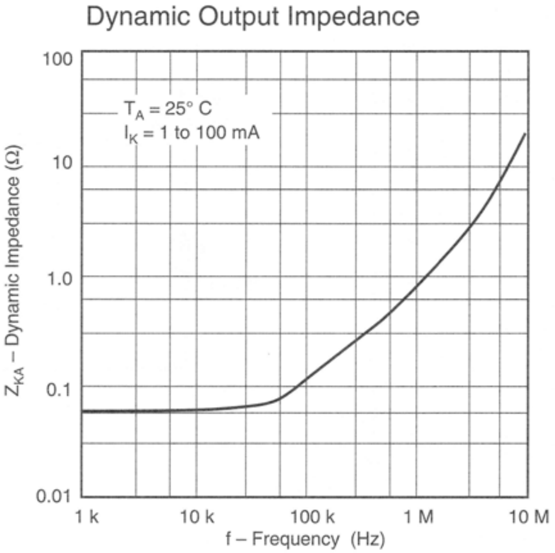


Figure 10

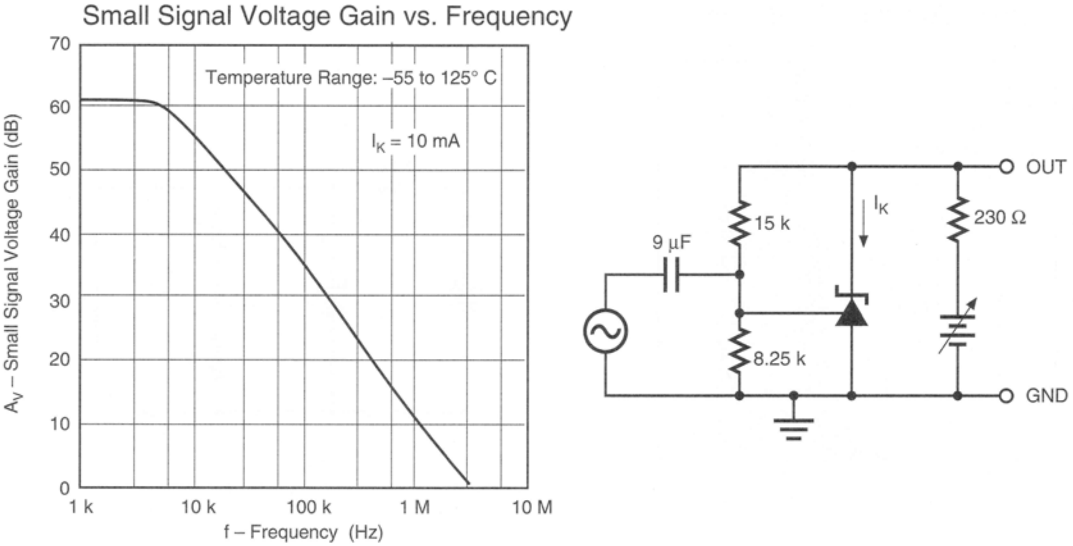


Figure 11

Typical Performance Curves

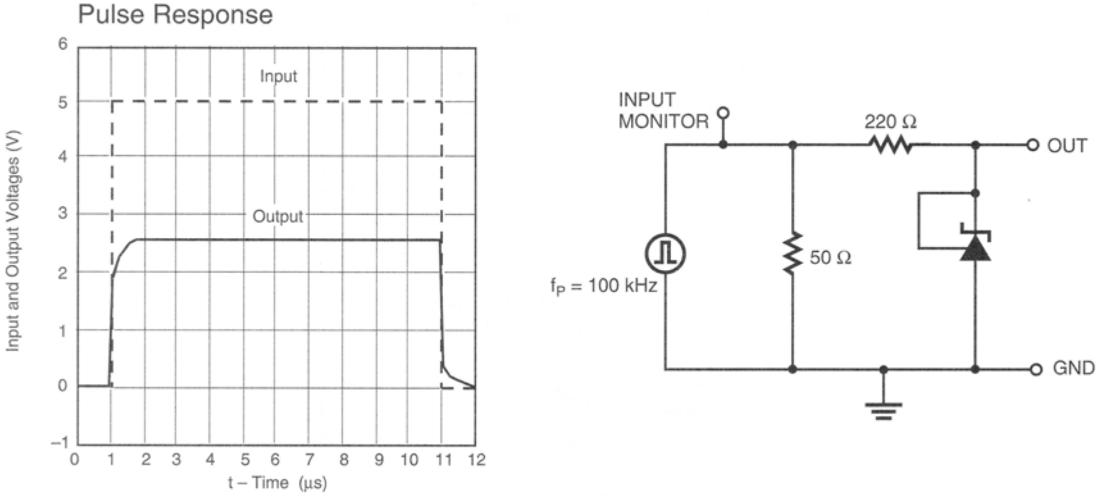


Figure 12

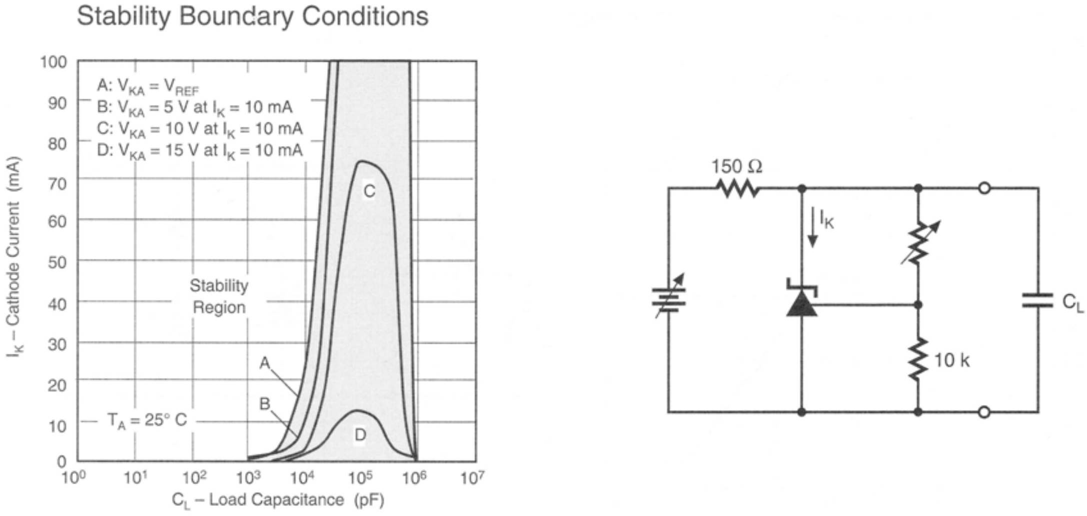
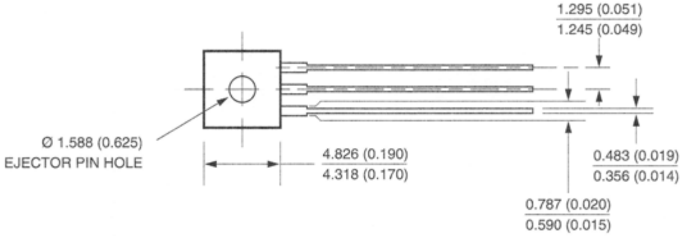


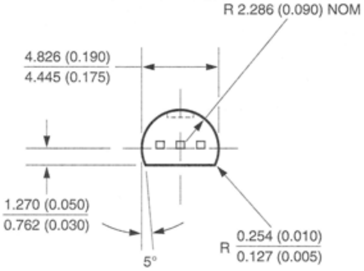
Figure 13

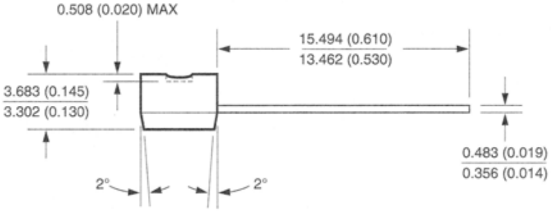
Package Dimensions

All Dimensions in mm (Inches)

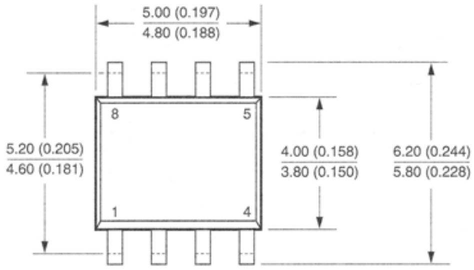
TO-92 Plastic (LP)

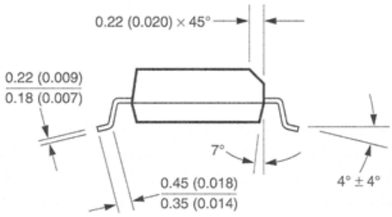


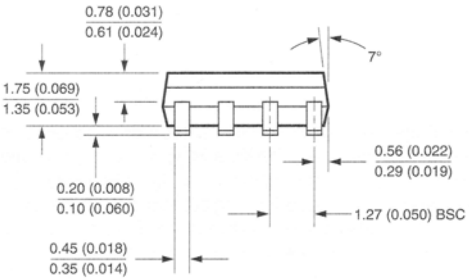




8-Pin Plastic SOIC (D)



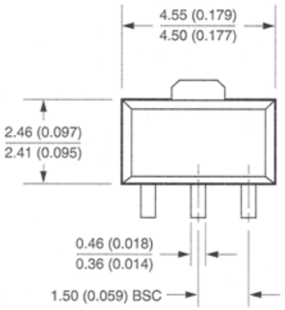


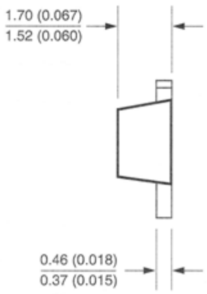


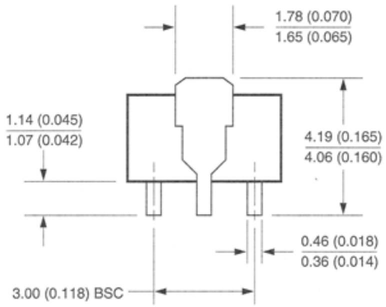
Package Dimensions

All Dimensions in mm (Inches)

SOT-89 (S)







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ASTEC SEMICONDUCTOR

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ASTEC

AS2431

Precision Adjustable Shunt Reference

Preliminary Specification

Features

- Temperature-compensated: 15 ppm/°C
- Trimmed 0.5% bandgap reference
- Internal amplifier with 100 mA capability
- Temperature range: Extended to 0 to 105° C
- Low frequency dynamic output impedance: < 150 mΩ
- Low output noise

Description

The AS2431 is a three-terminal adjustable shunt regulator providing a highly accurate 0.5% bandgap reference. The adjustable shunt regulator is ideal for a wide variety of linear applications that can be implemented using external components to obtain adjustable currents and voltages.

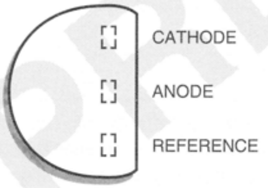
In the standard shunt configuration, the combination of low temperature coefficient (T.C.), sharp turn-on characteristics, low output impedance and programmable output voltage make this precision reference an excellent error amplifier.

The AS2431 is a direct replacement for the AS431 in low voltage, low current applications. It is also available in the very small footprint SOT-23.

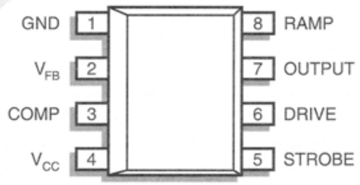
PRELIMINARY

Pin Configuration — Top view

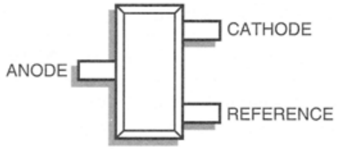
TO-92 (LP)



SOIC (D)



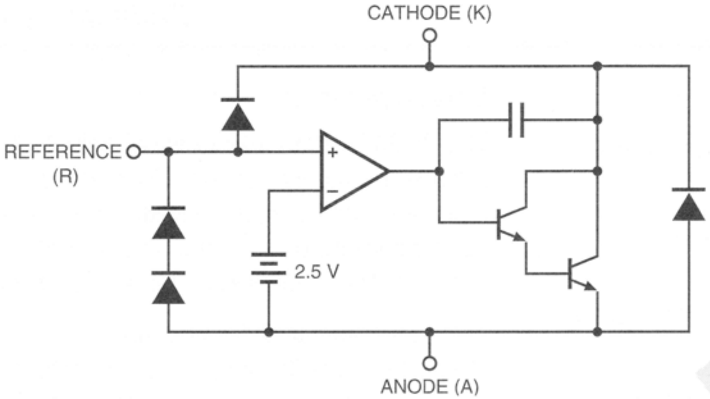
SOT-23 (VS)



Ordering Information

Description	Temperature Range	Order Codes
TO-92	0 to 105° C	AS2431LP
8-Pin Plastic SOIC	0 to 105° C	AS2431D
SOT-23	0 to 105° C	AS2431VS

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Cathode-Anode Reverse Breakdown	V_{KA}	20	V
Anode-Cathode Forward Current	I_{AK}	1	A
Operating Cathode Current	I_{KA}	100	mA
Reference Input Current	I_{REF}	1	mA
Continuous Power Dissipation at 25° C	P_D		
TO-92		775	mW
8L SOIC		750	mW
SOT-23		200	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	– 65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Cathode Voltage	V_{KA}	V_{REF} to 20	V
Cathode Current	I_K	10	mA

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160° C/W	80° C/W	6.3 mW/°C
SOIC	175° C/W	45° C/W	5.7 mW/°C
SOT-23	575° C/W	150° C/W	1.7 mW/°C

PRELIMINARY

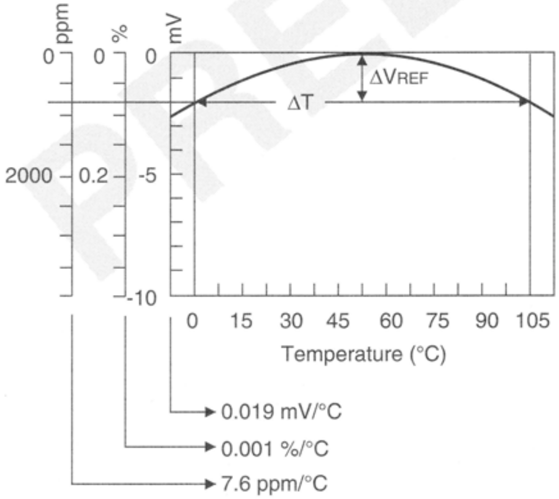
Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{KA} = V_{REF}$ and $I_K = 10$ mA unless otherwise stated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	Circuit
Reference Voltage	V_{REF}	$T_A = 25°$ C	2.490	2.500	2.510	V	1
		Over temp.	2.480	2.525	2.530	V	1
ΔV_{REF} with Temp*	TC			0.02	0.06	mV/ ° C	1
Ratio of Change in V_{REF} to Cathode Voltage	$\frac{\Delta V_{REF}}{\Delta V_K}$	V_{REF} to 10 V	– 2.7	– 1.01	– 2.7	mV/V	2
		10V to 20 V	– 2	– 0.4	0.3		
Reference Input Current	I_{REF}			0.7	4	µA	2
I_{REF} Temp Deviation	ΔI_{REF}	Over temp.		0.4	1.2	µA	2
Min I_K for Regulation	$I_{K(min)}$			0.4	1	mA	1
Off State Leakage	$I_{K(off)}$	$V_{REF} = 0$ V, $V_{KA} = 20$ V		0.04	500	nA	3
Dynamic Output Impedance	Z_{KA}	$f \leq 1$ kHz $I_K = 1$ to 50 mA		0.15	0.5	Ω	1

PRELIMINARY

*Calculating Average Temperature Coefficient (TC)



- $\text{TC in mV/°C} = \frac{\Delta V_{REF}}{\Delta T_A}$

- $\text{TC in \%/°C} = \frac{\left(\frac{\Delta V_{REF}}{V_{REF}\text{ at }25°\text{C}}\right) \times 100}{\Delta T_A}$

- $\text{TC in ppm/°C} = \frac{\left(\frac{\Delta V_{REF}}{V_{REF}\text{ at }25°\text{C}}\right) \times 10^6}{\Delta T_A}$

Test Circuits

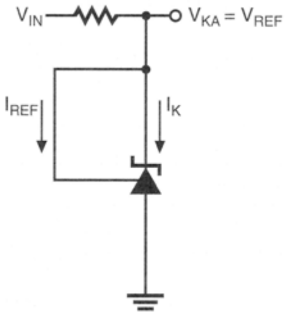


Figure 1a. Test Circuit 1

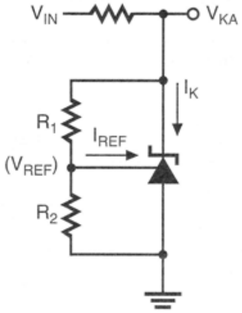


Figure 1b. Test Circuit 2

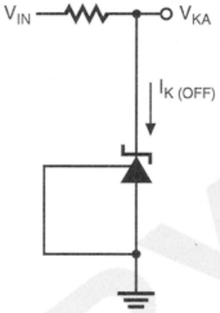


Figure 1c. Test Circuit 3

PRELIMINARY

Typical Performance Curves

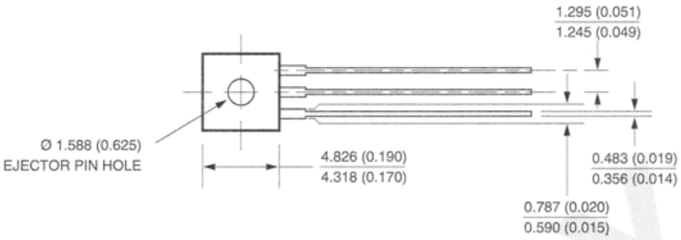
Not Available at Time of Publishing

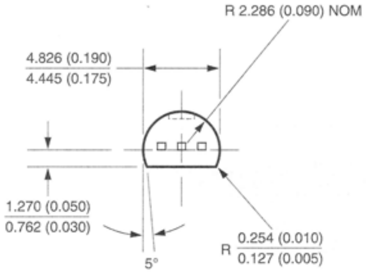
PRELIMINARY

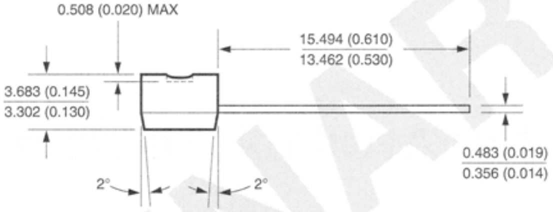
Package Dimensions

All Dimensions in mm (Inches)

TO-92 Plastic (LP)

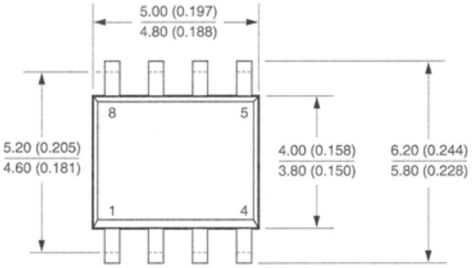


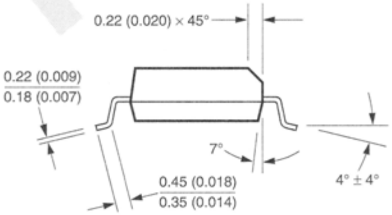


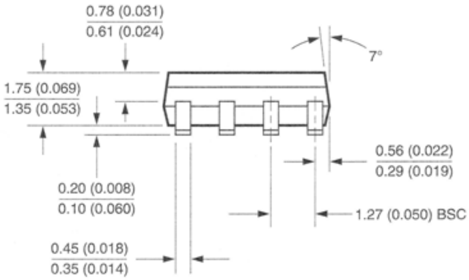


PRELIMINARY

8-Pin Plastic SOIC (D)



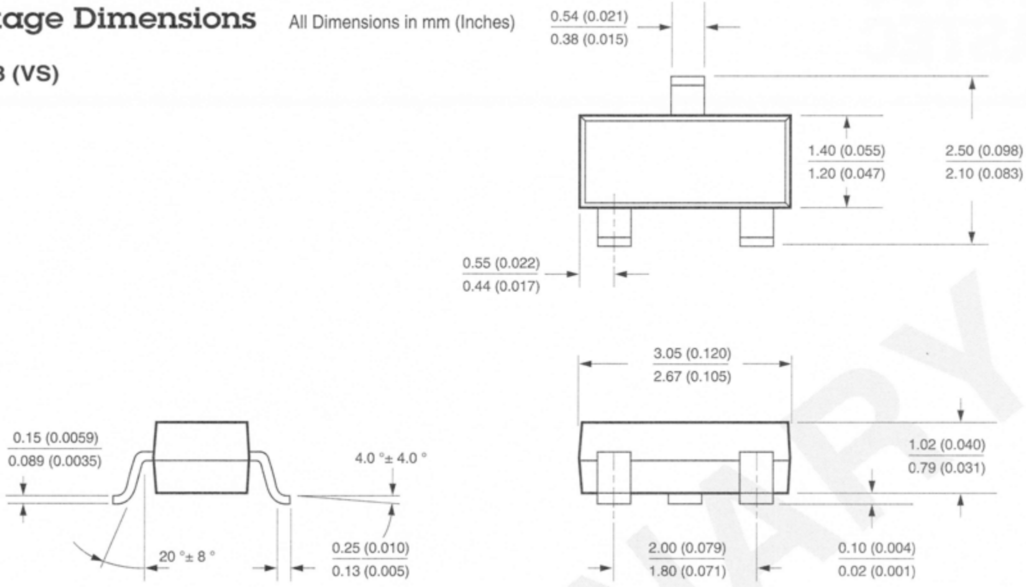




Package Dimensions

All Dimensions in mm (Inches)

SOT-23 (VS)



PRELIMINARY

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ASTEC SEMICONDUCTOR

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Notes

AS1004

Micropower Voltage Reference

Features

- Low voltage reference
- 10 µA turn-on current for AS1004-1.2
- 20 µA turn-on current for AS1004-2.5
- ± 4 mV (0.3 %) initial accuracy for AS1004-1.2
- ± 20 mV (0.3 %) initial accuracy for AS1004-2.5
- Guaranteed operation to 20 mA. Over three orders of magnitude of operating current!
- Temperature performance guaranteed
- Very low dynamic impedance

Description

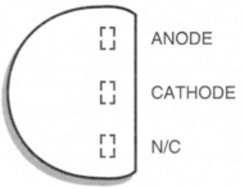
The AS1004 is a two-terminal precision band-gap voltage reference with a low turn-on current of 10 µA.

Emulating a 1.235 V zener diode, the AS1004 operates more than three orders of magnitude of output current with minute output impedance and guaranteed stability. With an initial tolerance of ± 4 mV and guaranteed temperature performance, it is ideal for precision instrumentation, especially in low power applications. Being a low-voltage reference, the AS1004 is also well-suited as a reference for low-voltage power supply applications, especially in power supplies intended for low-voltage logic systems, laptop computers and other portable or battery operated equipment.

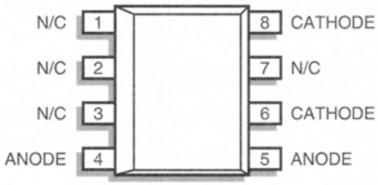
The AS1004 is pin-for-pin compatible with the LT1004 and the LM385 and offers improved specifications over both the LM385 and the MP5010. It is also available as a 2.5 V reference with a guaranteed start-up current of 20 µA.

Pin Configuration — Top view

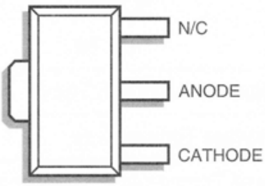
TO-92 (LP)



SOIC (D)



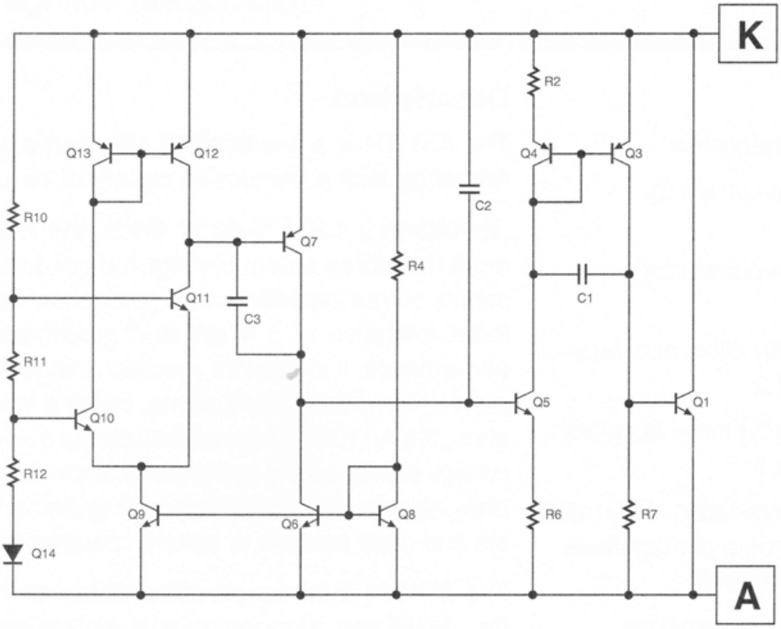
SOT-89 (S)



Ordering Information

Description	Temperature Range	Order Codes	
TO-92	0 to 70° C	AS1004-1.2LP	AS1004-2.5LP
8-Pin Plastic SOIC	0 to 70° C	AS1004-1.2D	AS1004-2.5D
SOT-89	0 to 70° C	AS1004-1.2S	AS1004-2.5S

Simplified Schematic



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Reverse Breakdown Current	I_Z	30	mA
Forward Current	I_F	30	mA
Continuous Power Dissipation at 25° C	P_D		
TO-92		775	mW
8LSOIC		750	mW
SOT-89		1000	mW
Maximum Junction Temp	T_J	150	°C
Storage Temperature	T_{STG}	–65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Recommended Conditions

Parameter	Symbol	Rating	Unit
Cathode Current	I_Z	100	µA

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160° C/W	80° C/W	6.3 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C
SOT-89	110° C/W	8° C/W	9.1 mW/°C

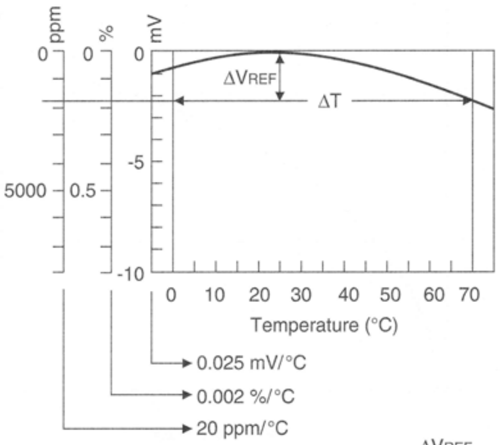
Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (0 to 70° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics.

Parameter	Symbol	Test Condition	AS1004-1.2			AS1004-2.5			Unit
			Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	V_Z	$I_Z = 100\ \mu A$, $T_J = 25°$ C	1.231	1.235	1.239	2.480	2.500	2.520	V
		$0°\ C \le T_A \le 70°$ C	1.225	1.235	1.245	2.470	2.500	2.530	V
Average Temperature Coefficient	$\Delta V_Z / \Delta T$	$I_{min} \le I_Z \le 20$ mA		20			60		ppm/°C
Minimum Operating Current	$I_{Z\,(min)}$			4	10		12	20	µA
Reverse Breakdown Voltage Change With Current	$\Delta V_Z / \Delta I_Z$	$I_{min} \le I_Z \le 1$ mA		0.5	1		0.5	1	mV
		Over Temperature		0.5	1.5		0.5	1.5	mV
		$1\ mA \le I_Z \le 20$ mA		6.5	10		6.5	10	mV
		Over Temperature		6.5	20		6.5	20	mV
Reverse Dynamic Impedance	Z_Z	$I_Z = 100$ mA, f = 25 Hz		0.2	0.6		0.8	0.9	Ω
		Over Temperature		1	1.5			1.5	Ω
Wide Band Noise	e_n	$I_Z = 100\ \mu A$ $10\ Hz \le f \le 10$ KHz		60			60		µV
Long Term Stability	$\Delta V_Z / \Delta T$	$I_Z = 100\ \mu A$ $T_A = 25°\ C \pm 0.1°$ C		20			60		ppm/kH

Typical Performance Curves

Calculating Average Temperature Coefficient for the AS1004-1.2 Reference



$$\text{Average Temperature Coefficient} = \frac{\Delta V_{REF}}{\Delta T}$$

Figure 1

AS1004-1.2 Reference Voltage vs. Ambient Temperature

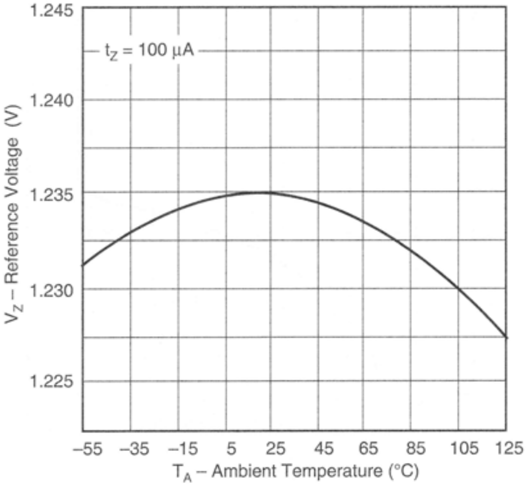


Figure 2

Typical Performance Curves

Calculating Average Temperature Coefficient for the AS1004-2.5 Reference

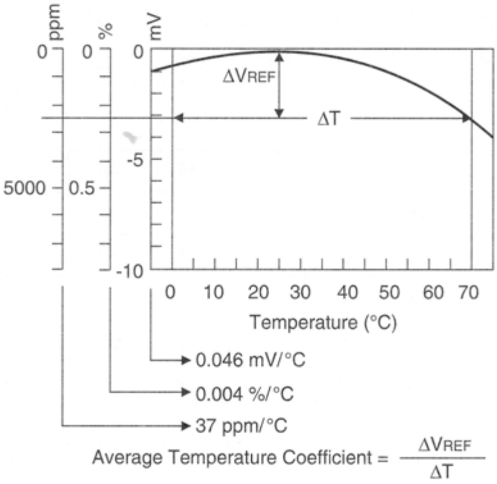


Figure 3

AS1004-2.5 Reference Voltage versus Ambient Temperature

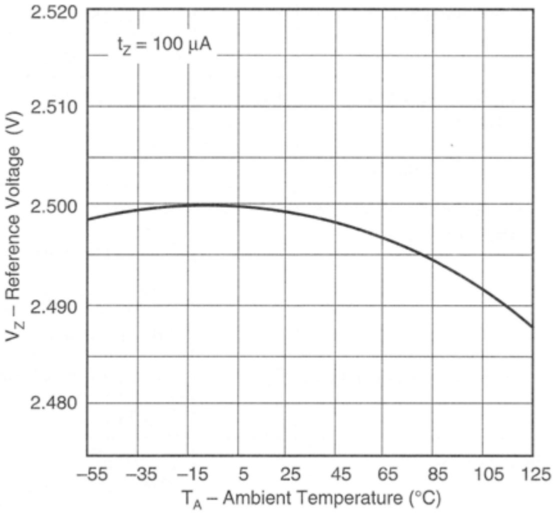


Figure 4

AS1004-1.2 Reverse Operating Characteristics

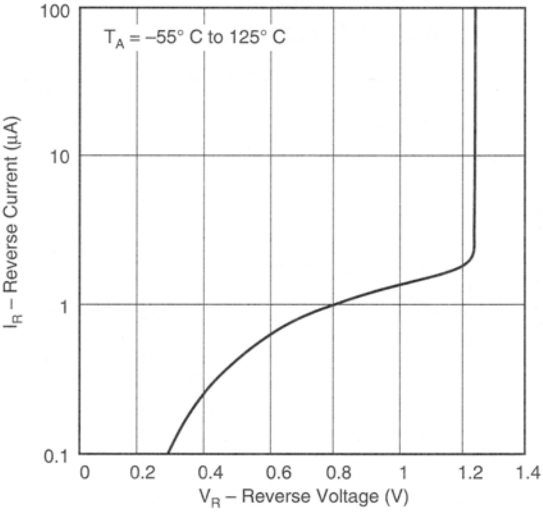


Figure 5

AS1004-2.5 Reverse Operating Characteristics

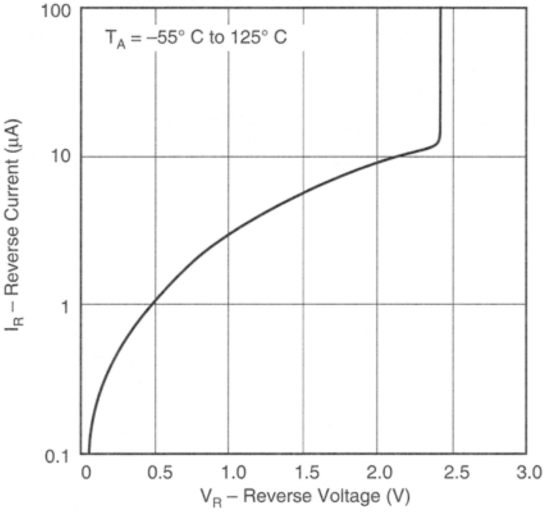


Figure 6

Typical Performance Curves

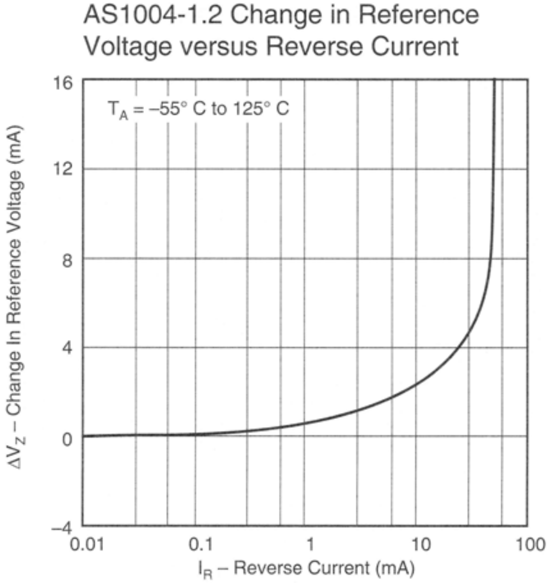

AS1004-1.2 Change in Reference Voltage versus Reverse Current

Figure 7

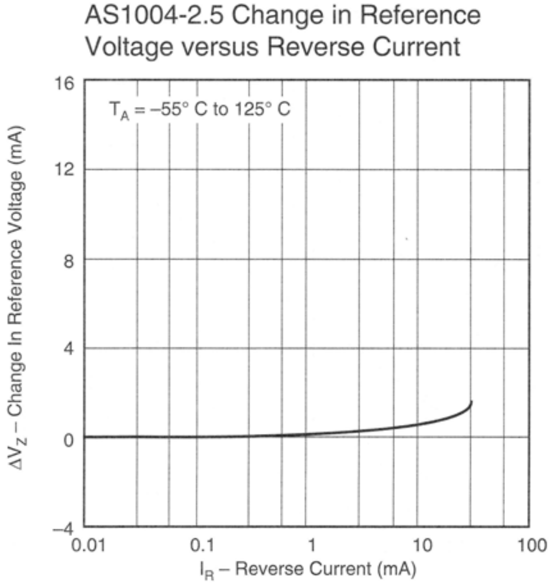

AS1004-2.5 Change in Reference Voltage versus Reverse Current

Figure 8

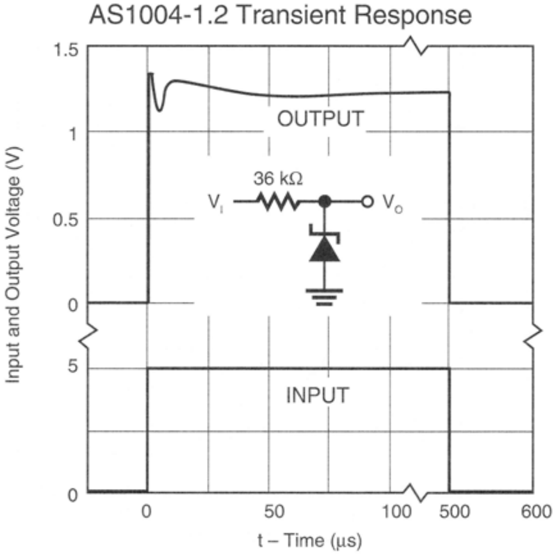

AS1004-1.2 Transient Response

Figure 9

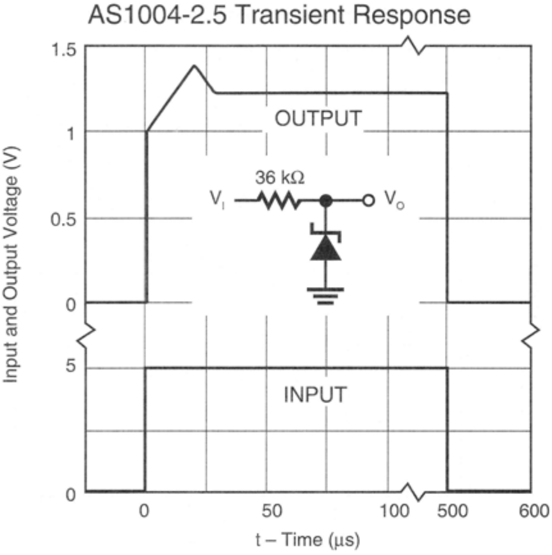

AS1004-2.5 Transient Response

Figure 10

Typical Performance Curves

AS1004-1.2 Reverse Dynamic Impedance

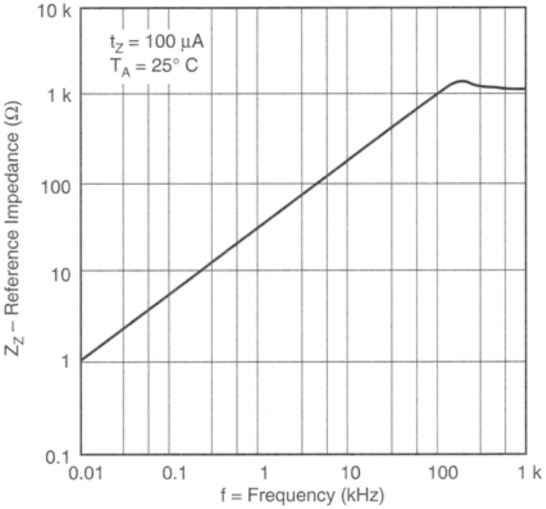


Figure 11

AS1004-2.5 Reverse Dynamic Impedance

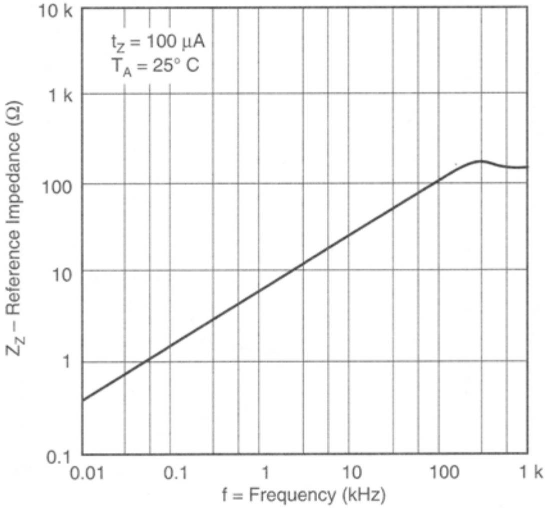


Figure 12

Forward Characteristics

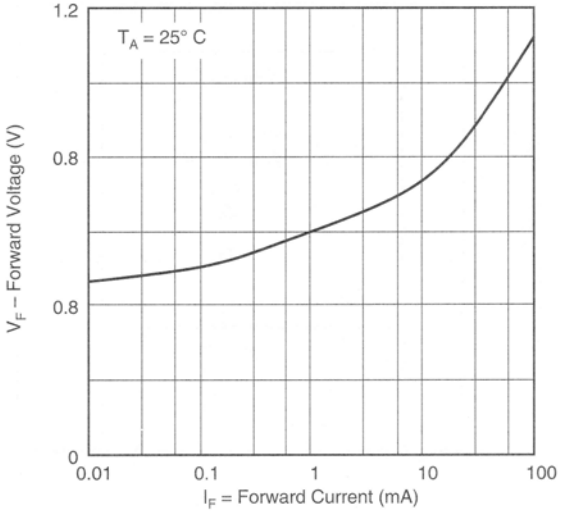


Figure 13

Low Frequency Reverse Dynamic Impedance

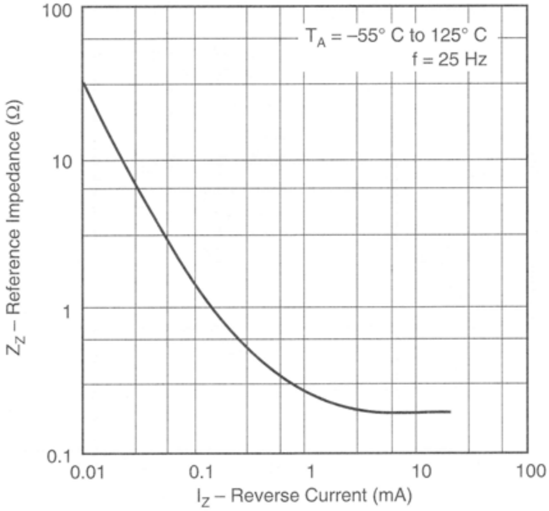


Figure 14

Typical Applications

1.235V Reference

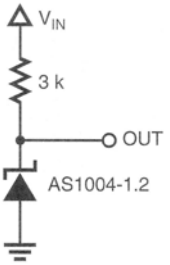


Figure 15

2.5V Reference

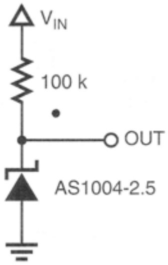


Figure 16

Low Noise Reference

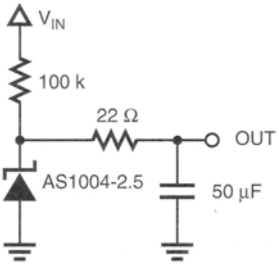


Figure 17

Variable Output Regulator

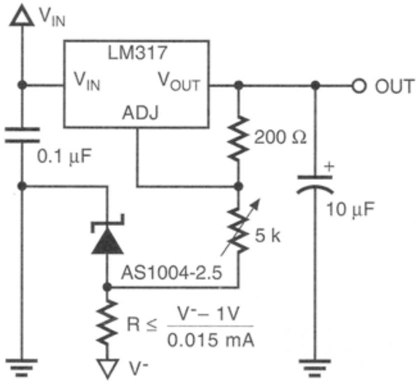


Figure 18

High Stability 5V Regulator

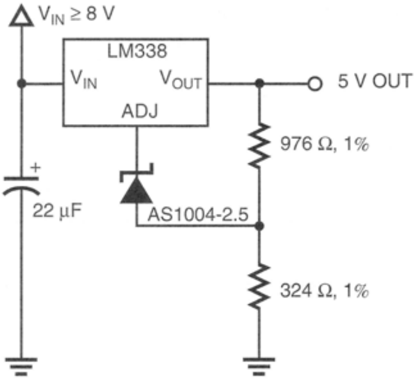


Figure 19

Lead Acid Low Battery Detector

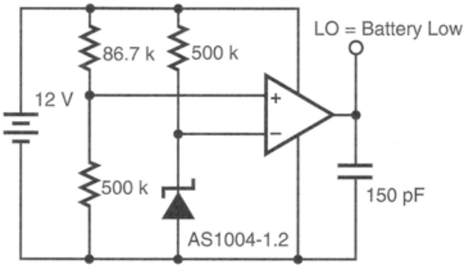


Figure 20

Micropower 10V Reference

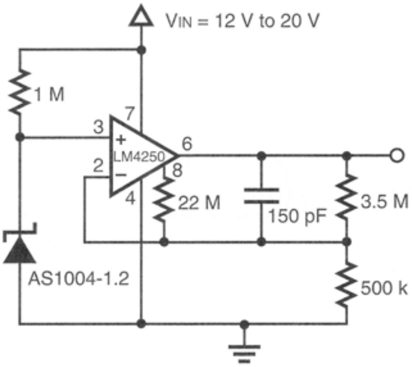
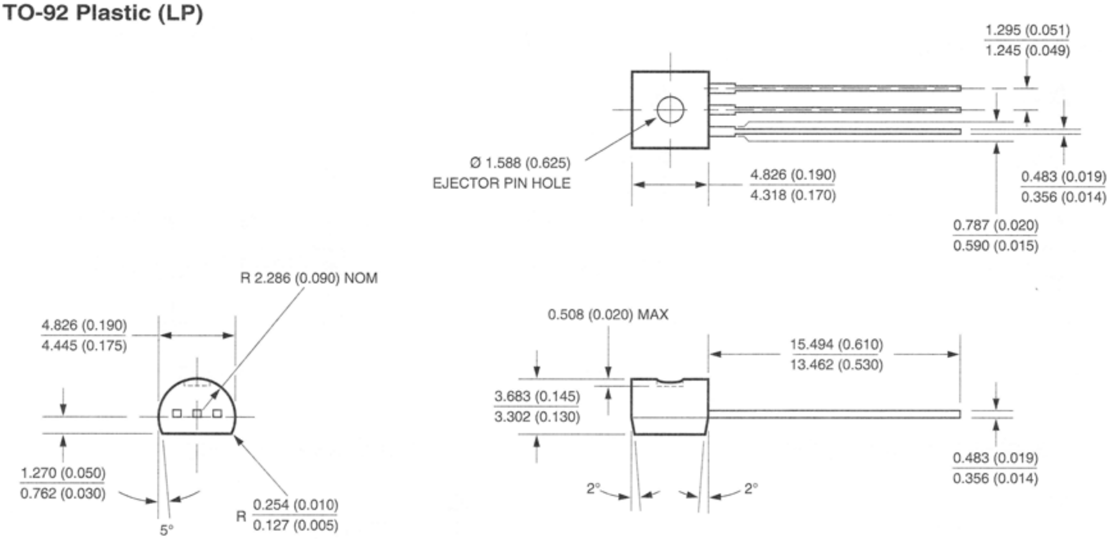


Figure 21

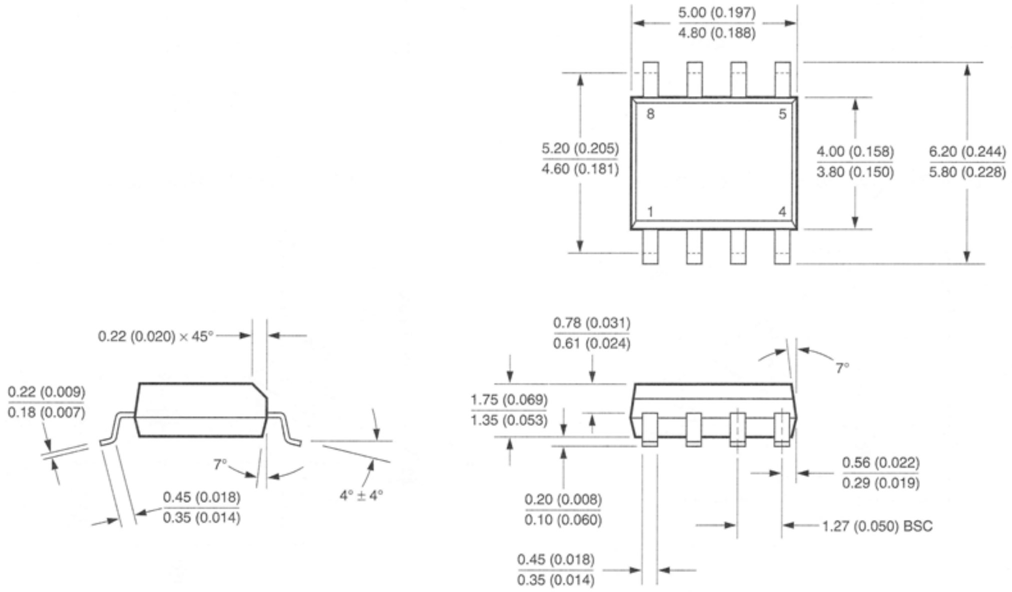
Package Dimensions

All Dimensions in mm (inches)

TO-92 Plastic (LP)

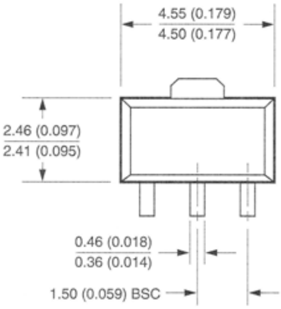


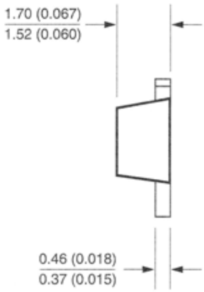
8-Pin Plastic SOIC (D)

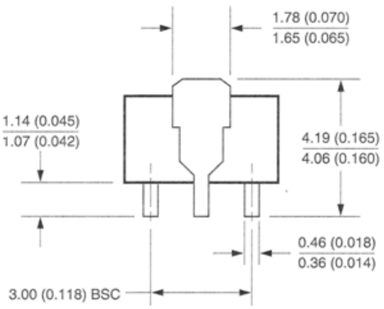


Package Dimensions All Dimensions in mm (inches)

SOT-89 (S)







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Notes

ASTEC

AS1012

High Frequency PWM Controller

Features

- All parameters specified at 500 kHz
- Internal high-speed logic
- Remote on/off control
- Feed-foward control
- External synchronization
- Adjustable UVLO
- Soft-start
- Trimmed and temperature-compensated 1% bandgap reference
- Operates in voltage or current mode
- Current limit with both inputs available and 12 V common mode
- Over-temperature shutdown

Description

The AS1012 is a full-featured, general purpose PWM controller. Intended for use in single ended high frequency switching power supplies, the AS1012 can implement either traditional voltage controlled or the newer current mode control schemes. Although usable over a wide range of frequencies, this circuit is designed specifically for use at 500 kHz.

The AS1012 has an exceptionally flexible architecture, with an internal 2.5 V bandgap reference trimmed to 1% precision. It also has a completely uncommitted 7 MHz op amp available for a loop amplifier, a high-speed oscillator with a feedforward input that varies the oscillator amplitude for providing open loop line regulation and eliminates loop gain modulation in voltage mode configurations.

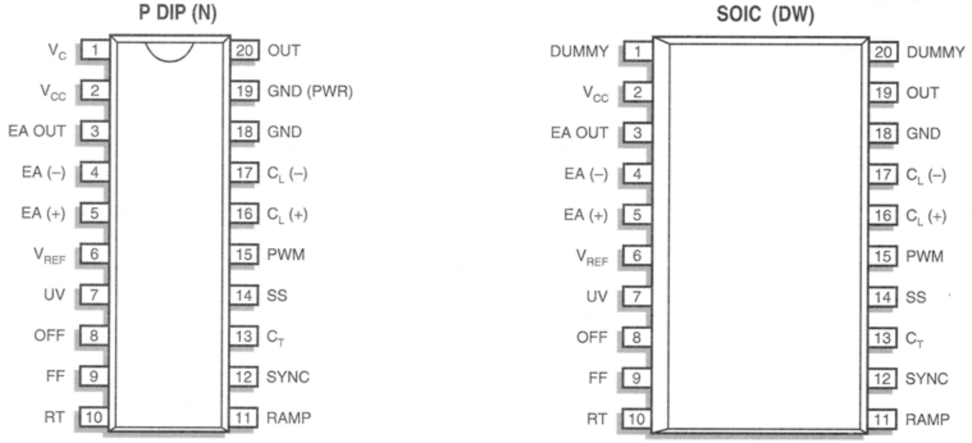
The PWM function is performed by either the PWM comparator or the Current Limit comparator, which are actually general purpose high-speed comparators, both functioning to control pulse width. The output stage is a high current totem pole output. This is designed to drive large MOSFETs and includes an internal voltage clamp that prevents overdriving the FET gate independent of chip V_{CC}.

Several advanced features are also provided in the AS1012. There is a synchronization input allowing for running off of an external clock. The under-voltage lockout is programmable and toggles the chip in and out of a low current (1 mA) start-up mode. A remote on/off function or the overtemperature circuit can also toggle the chip into this low current mode. A soft-start function is built into the PWM comparator.

Ordering Information

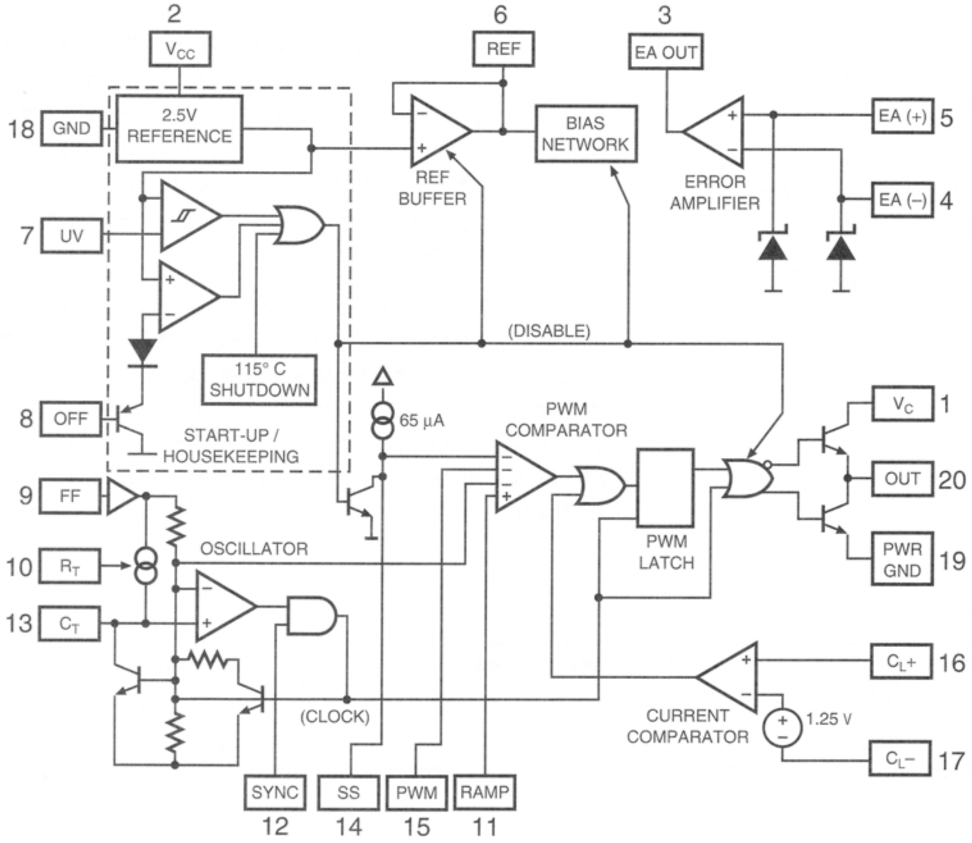
Description	Temperature Range	Order Codes
20-Pin Plastic DIP	0 to 85° C	AS1012N
20-Pin Plastic SOIC	0 to 85° C	AS1012DW

Pin Configuration — Top view


P DIP (N)

SOIC (DW)

Functional Block Diagram



Pin Function Description

Pin Number		Function	Description
DIP	SOIC		
1	–	V_C	Separate positive voltage for the Output. Only available in PDIP package.
2	2	V_{CC}	Positive supply voltage for the IC. This voltage may be between 7 V and 20 V.
3	3	EA OUT	Output of the Error Amplifier. This is an NPN emitter follower with a fixed current source pull-down.
4	4	EA–	Inverting Error Amp input. This is an NPN input clamped with a 5.6 V zerner to ground.
5	5	EA+	Non-inverting Error Amp input. This also is an NPN input clamped with a 5.6 V zener to ground.
6	6	V_{REF}	Output of the 2.5 V bandgap reference. This is a low current reference and should not be significantly loaded or directly decoupled.
7	7	UV	The under-voltage lockout input. The chip remains in the "off" state until this pin is raised above 2.5 V, and remains "on" until UV drops below 2 V. This is programmed by an external resistor divider from V_{CC} or the bulk supply.
8	8	OFF	External remote on/off input. When high (TTL logic levels), this impedance input puts the chip in its low current "off" mode. When open, this pin defaults high.
9	9	FF	Oscillator Feed Forward input. This pin scales the amplitude of the oscillator signal. When open, this pin defaults high.
10	10	R_T	Timing resistor input. An external resistor to ground sets the oscillator charge current ($I_{CT} = V_{FF}/R_T$). A value of 3.9 kΩ is typically optimum for minimizing temperature and line regulation of frequency.
11	11	RAMP	Non-inverting PWM comparator input. This pin typically used with a positive going ramp voltage either from the oscillator for voltage mode control, or a current derived ramp for current mode control. When V_{RAMP} exceeds either V_{PWM} or V_{SS} the current output pulse is terminated.
12	12	SYNC	Synchronization input. When low, this high impedance input disables the oscillator discharge, therefore lowering oscillator frequency.
13	13	C_T	Oscillator capacitor. With a 3.9 kΩ R_T, C_T is approximately $C_T = (4{,}250\ f_{OSC})^{-1}$.
14	14	SS	Soft-Start input. This input to the PWM comparator is identical to the PWM pin, except that a current source has been added to allow for a soft-start function. If this pin is connected to an external capacitor, the 65 µA current source will gradually charge the capacitor, continuously varying the duty cycle. In the low current "off" mode, this pin is pulled active low to reset the soft-start capacitor.
15	15	PWM	Inverting input to the PWM comparator. This input, along with SS, is compared to the RAMP input. When V_{RAMP} exceeds either V_{PWM} or V_{SS} the current output pulse is terminated.
16	16	CL+	Positive Current Limit comparator input. When CL (+) input is greater than 1.25 V above CL (–) input, the current output pulse is terminated.
17	17	CL–	Negative Current Limit comparator input.
18	18	GND	Analog ground and IC substrate.
19	–	Power GND	Separate output ground. Available in PDIP package only.
20	19	OUT	Output of PWM circuitry. Designed to directly drive N-channel MOSFETs with loading limited only by power dissipation considerations ($P = C_{LOAD}\ (V_{CC})^2\ f_{OSC}$).
	1, 20	N/C	No connection. To allow for 18L SOP-W compatibility.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage	V_{CC}	20	V
Supply Voltage (power out)	V_C	20	V
Error Amplifier Inputs	EA+, EA–	5	V
Reference Sink Current	I_{REF}	100	mA
Synchronization Input	V_{SYNC}	30	V
Remote on/off Input	V_{OFF}	30	V
Under-voltage Lockout Input	V_{UV}	30	V
PWM Comparator Input	V_{PWM}	30	V
RAMP Comparator Input	V_{RAMP}	30	V
Operating Frequency	f_{OP}	1.5	MHz
Continuous Power at 25° C	P_D		
20L PDIP		1000	mW
20LSOIC		1000	mW
Ambient Temperature	T_A	85	°C
Junction Temperature (self-limiting)	T_J	115	°C
Storage Temperature	T_{STG}	–65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	7 to 20	V
Output Supply	V_C	7 to 20	V
Operating Frequency	f_{OP}	10 to 500	kHz

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
20 L PDIP	60° C/W	24° C/W	16.6 mW/°C
20 L SOP-W	85° C/W	25° C/W	11.8 mW/°C

Electrical Characteristics

Electrical characteristics are guaranteed over full junction temperature range (0 to 85° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{CC} = 20$ V, $C_T = 470$ pF and $R_T = 3.9$ kΩ unless otherwise stated.

Parameter	Symbol	Test Condition	AS1012 Min	 Typ	 Max	Unit
Reference						
Output Voltage	V_{REF}	$I_{REF} = 1$ mA	2.550	2.575	2.600	V
Line Regulation		6 V < V_{CC} < 20 V		5	10	mV
Load Regulation		0.5 < I_{REF} < 5 mA		5	20	mV
Temperature Stability[1]	TC			0.1	0.19	mV/°C
Short Circuit Current	I_{SC}	$V_{REF} = 0$ V	6	12		mA
Oscillator						
Initial Accuracy	f_{OSC}	$R_T = 3.9$ kΩ, $C_T = 470$ pF	450	500	550	kHz
Line Stability		10 V < V_{CC} < 20 V		2	4	%
Feed-Forward Stability		6 V < FF < 20 V		4		%
Temperature Stability				4		%
Dead Time				100		ns
Amplitude		FF = 15 V	10	12	14	V
Sync Threshold			0.8	1.4	2.0	V
Maximum Range				1.5		MHz
Error Amplifier						
Input Offset Voltage		$EA_{OUT} = 2.5$ V		2	7	mV
Input Bias Current		$V_{IN} = 2.5$ V		0.12	1.8	μA
V_{OUT} High	V_{OH}	$R_L = 2$ kΩ	12	17		V
V_{OUT} Low	V_{OL}	$R_L = 2$ kΩ		50	100	mV
Input Range			1.2		3.8	V
Open Loop Gain	A_{VOL}	$R_L = 10$ MΩ		95		dB
Open Loop Gain	A_{VOL}	$R_L = 10$ kΩ	60	75		dB
Gain Bandwidth Product	GBW			5		MHz
Power Supply Rejection Ratio	PSRR			80		dB
Output Source Current	I_{SOURCE}		5	10		mA
Output Sink Current	I_{SINK}		0.4	1.0		mA
Output Impedance	Z_O	$R_L = 1$ kΩ		1		Ω
Slew Rate	SR			1.9		V/μs

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 85° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{CC} = 20$ V, $C_T = 470$ pF and $R_T = 3.9$ kΩ unless otherwise stated.

Parameter	Symbol	Test Condition	AS1012 Min	 Typ	 Max	Unit
PWM Comparator						
Minimum Duty Cycle[2]					2	%
Minimum Off Time				200	300	ns
PWM Input Bias Current	$I_{BIAS\ PWM}$	PWM < RAMP, SS	–10	– 4	0	µA
RAMP Input Bias Current	$I_{BIAS\ RAMP}$	RAMP < PWM, SS	–10	–2	0	µA
Soft-Start Input Bias	$I_{BIAS\ SS}$	SS < PWM, RAMP	–100	–65	–25	µA
Common-mode Input Range			–0.1		12	V
Differential-mode Input Range			– 0.3		40	V
Propagation Delay to Output	t_{PD}			105		ns
Current Limit						
Offset Voltage	$V_{OS\ CL}$		1.2	1.27	1.35	V
Common-mode Input Range			–0.1		12	V
Input Bias Current			–15	–3	0	µA
Propagation Delay to Output	t_{PD}			125		ns
Housekeeping						
Under-voltage ON Threshold	UV_{ON}	V_{CC} Raised From 1 V	2.5	2.6	2.7	V
Under-voltage OFF Threshold	UV_{OFF}	V_{CC} Lowered From 13 V	1.85	2.0	2.1	V
Under-voltage Hysteresis			22	26	30	%
Under-voltage Bias Current	$I_{BIAS\ UV}$		–1.5	–0.1	0	µA
Remote ON/OFF Threshold		Circuit Off	0.8	1.4	2.0	V
Remote ON/OFF Bias Current	$I_{BIAS\ OFF}$		–1.5	–0.1	0	µA
Output Stage						
V_{OUT} High[3]	V_{OH}	$I_O = 10$ mA	13	15.0	16	V
		$I_O = 200$ mA	12	14.5	16	V
V_{OUT} Low	V_{OL}	$I_O = 10$ mA		1.0	2	V
		$I_O = 200$ mA		1.0	2	V
Rise Time	t_R	$C_L = 1$ nF		35	70	ns
Fall Time	t_F	$C_L = 1$ nF		35	70	ns

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 85° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{CC} = 20$ V, $C_T = 470$ pF and $R_T = 3.9$ kΩ unless otherwise stated.

Parameter	Symbol	Test Condition	AS1012 Min	 Typ	 Max	Unit
Supply Current						
I_{CC} on[4]		$V_{CC} \leq 20$ V		10	15	mA
I_{CC} off[5]		$V_{CC} \leq 20$V		0.6	1.5	mA

Notes:

1. Temperature accuracy is the total deviation (maximum to minimum over the specified temperature range. For example, over the range 0 to 70°, the total allowable shift would be 5,250 ppm (13 mV).
2. The duty cycle is generally continuously variable to any arbitrary low value. The actual limiting factor for low duty cycle is generally a trapezoidal waveform (eventually triangular) at the output due to finite rise and fall time.
3. For $V_{CC} > 15$ V, the output stage clamps itself to avoid excessive voltages on the gates of power FETs and to limit the transfer of energy to gate capacitance beyond that required for switching.
4. Supply current rated as inherent chip drain only. Oscillator draws current under load. At 500 kHz into 1 nF gate capacitance, 35 mA is typical.
5. "OFF" supply current refers to either of two conditions:
    1. UV in low voltage range (under ≈2.5 V).
    2. OFF pin held high (TTL levels).

Typical Performance Curves

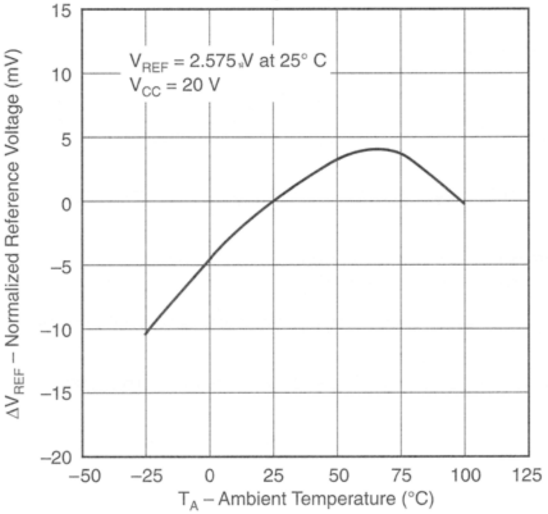

Temperature Coefficient of Reference Voltage

Figure 1

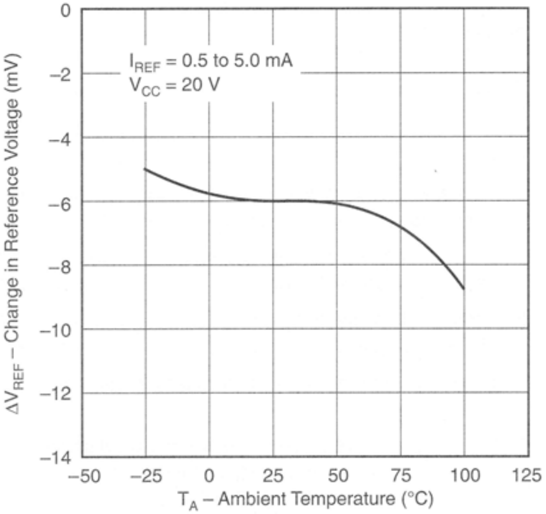

Reference Voltage Load Regulation

Figure 2

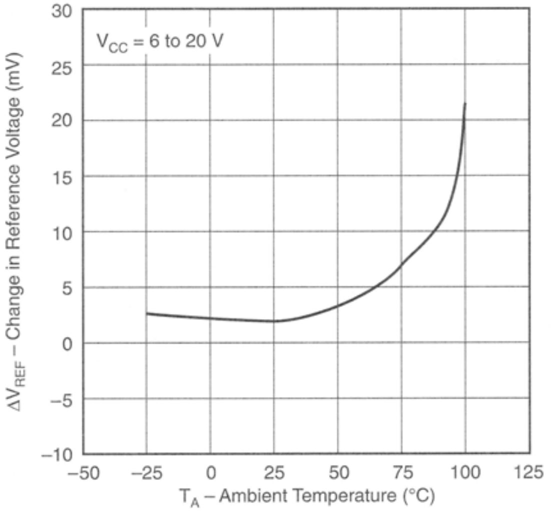

Reference Voltage Line Regulation

Figure 3

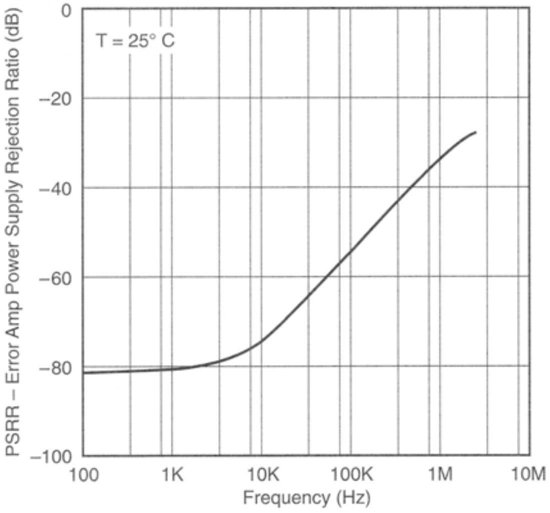

Power Supply Rejection Ratio of the Error Amplifier

Figure 4

Typical Performance Curves

Error Amplifier

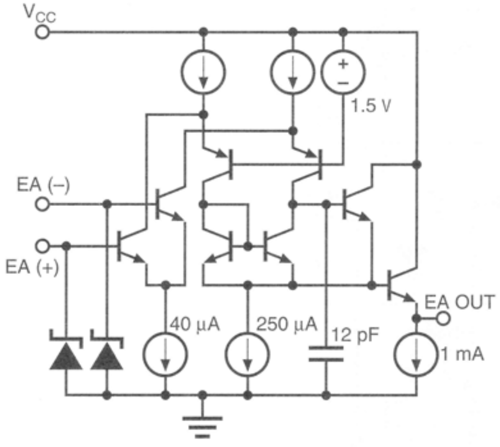


Figure 5

Dynamic Output Impedance of the Error Amplifier

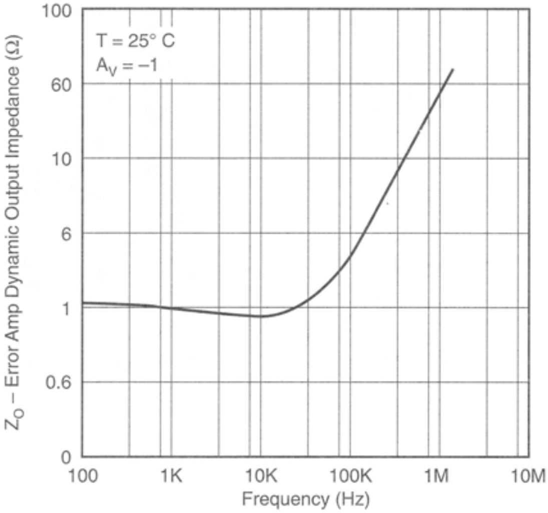


Figure 6

Error Amplifier Open Loop Frequency Response

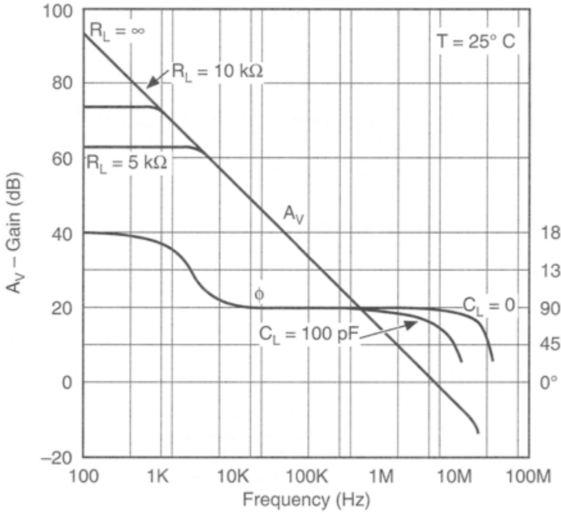


Figure 7

Error Amplifier Unity Gain Slew Rate

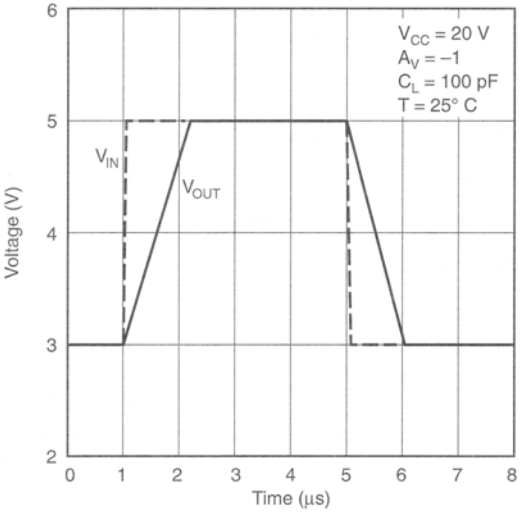


Figure 8

Typical Performance Curves

Oscillator

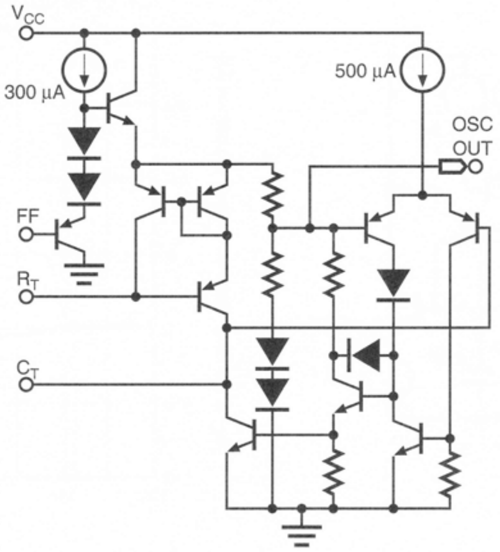


Figure 9

Feed Forward Voltage Temperature Stability

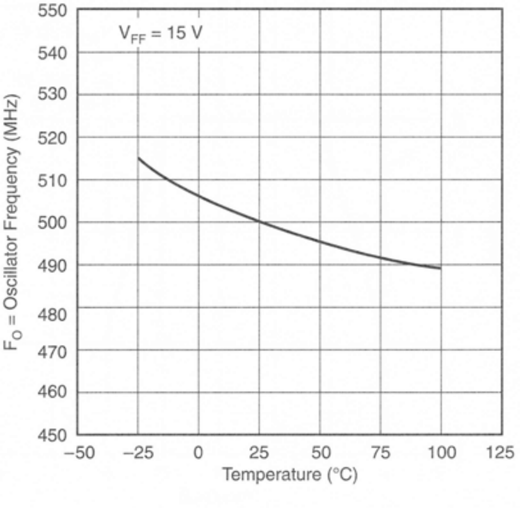


Figure 10

Oscillator Characteristics with Varying Feed Forward Voltage

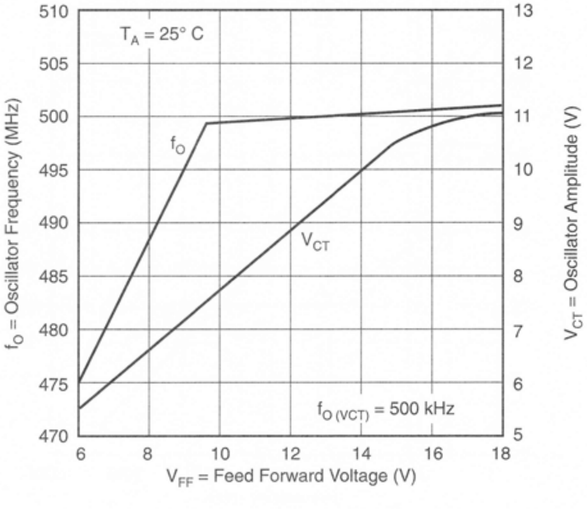


Figure 11

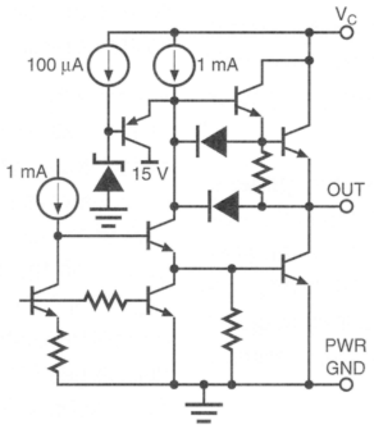

Output Stage

Figure 12

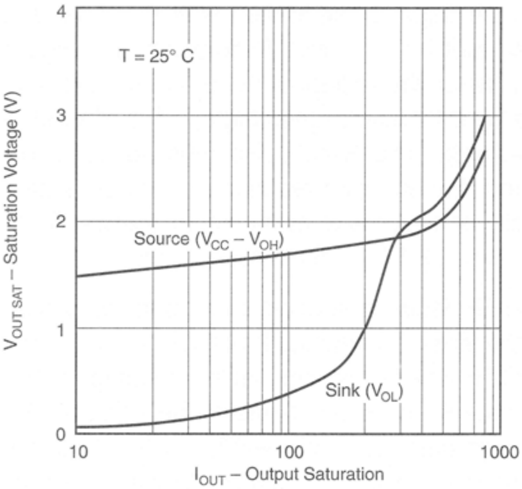

Output Saturation

Figure 13

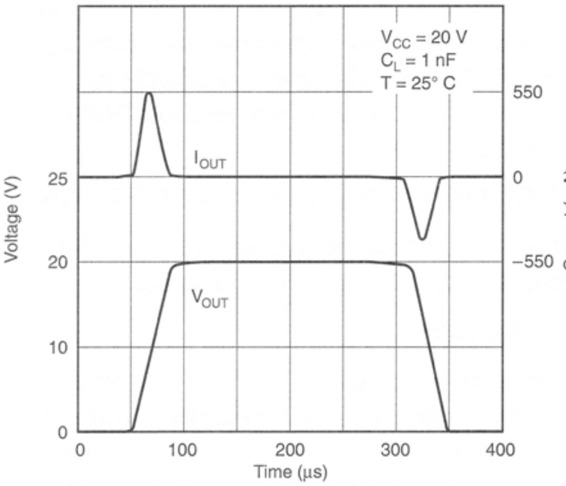

Output Saturation

Figure 14

Operating Description

A full-featured switch mode power supply (SMPS) control IC, the AS1012 is optimized for high frequency PWM power converters and can control both voltage mode and current mode converters. The AS1012 contains numerous other housekeeping functions, making it an "universal" control IC, adaptable to a wide variety of power control schemes.

Although this is a comprehensive and general description of the AS1012, its functions and applications, it should be understood the examples given do not limit the use of the AS1012 to any one topology or control scheme. Nor do they suggest that any given topology is preferred over another.

GENERAL OVERVIEW

The AS1012 was designed to be a universal SMPS controller. This is evident by viewing the block diagram. Several functional blocks (e.g. the error amplifier, PWM and current limit comparators) are uncommitted and a full range of housekeeping functions are included. The AS1012 is capable of controlling virtually any single-ended power converter topology, as well as power factor correction (PFC) preregulators and resonant converters. Although designed specifically for use at 500 kHz and below, operation above 500 kHz is possible.

SECTION 1—THEORY OF OPERATION

The following sections describe each of the functional blocks, their operation and limitations.

1.1 Oscillator

The oscillator section of the AS1012 provides both the system clock and a linear ramp (sawtooth) voltage waveform. The clock is internal to the IC and is used to set the frequency and timing for the internal logic. The ramp waveform (available at the CT pin) can be used as a reference for the PWM comparator in voltage mode control applications, or for slope compensation in current mode control. The pins associated with the oscillator are RT (pin 10), CT (pin 13), FF (pin 9) and SYNC (pin 12). Refer to section 2.3 for details on using the ramp for voltage or current mode control.

An external resistor (RT) sets the charge current in the external capacitor (CT), which sets the ramp slope. These are timing components that determine frequency. The upper and lower thresholds of the ramp generator are set by an internal divider off the FF pin. When the voltage across capacitor CT reaches the upper threshold, a high current transistor within the IC turns on and quickly discharges CT to the lower threshold. The cycle then repeats. Refer to section 2.1.1 for selection of RT and CT.

The SYNC pin provides a means for synchronizing the oscillator to an external clock. For synchronization, the oscillator's natural frequency is initially set slightly higher than the Sync frequency. Synchronization is activated by holding the SYNC pin low at the beginning of a cycle. This allows the ramp voltage to rise to the upper threshold and then wait for a positive Sync pulse (see Figure 15). When the voltage at the SYNC pin exceeds the Sync threshold (goes high), CT is allowed to discharge. The Sync pulse must then go low before the oscillator reaches the end of its next cycle, or it reverts to its natural frequency. Refer to section 2.1.2 for Sync applications.

The FF (feed-forward) pin controls the amplitude of the ramp. The amplitude of the ramp waveform at CT is directly proportional to the voltage at FF. If the FF pin is left floating, the effective FF voltage defaults to V_{CC}—2Vbe. If tied to a line dependent voltage, the amplitude of the ramp will track FF to provide a feedforward (open loop line regulation) function. Refer to section 2.1.3 for details on Feedforward.

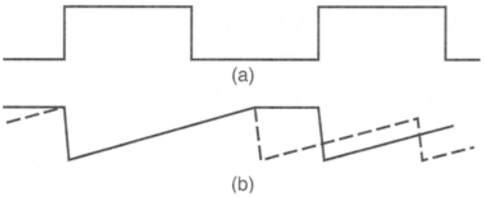


Figure 15. Sync and Oscillator Waveforms

Sync Signal (a) applied to pin 12 controls the oscillator ramp waveform (b) at pin 13. Dotted line shows the natural oscillator frequency.

Note: *The term "ramp" as used in this section refers to the sawtooth waveform present at the CT pin. This is not to be confused with the RAMP pin of the IC as discussed in section 1.4.*

The nature of the oscillator design allows it to be constant frequency/constant amplitude, AM modulated, FM modulated or both by controlling the RT, FF and SYNC inputs.

1.2 Reference

The voltage reference of the AS1012 is a trimmed, temperature compensated 2.5 volt bandgap with an initial accuracy of 1% and near zero TC over the normal operating temperature range. This reference serves a number of functions. Its primary purpose is to provide a precise voltage reference for the power supply system. This voltage is available at the V_{REF} pin (pin 6). In addition, the reference provides the DC bias for much of the IC's internal circuitry and is used for the various housekeeping functions.

The reference is divided into two sections. The first is a self-starting low current bandgap that remains active during all conditions and provides an internal reference to the UVLO (under-voltage lockout) and OFF circuitry. The second is a gated buffer circuit, which provides the internal DC bias for the rest of the IC's circuitry and the 2.5 volt V_{REF} to the outside world. The buffer is turned off during shutdown conditions in order to achieve a very low idle current ($\leq$1 mA). This, in conjunction with the UVLO circuitry, allows bootstrapping. The reference output is current limited to about 10 mA and is intended to be a source but not sink output. It should not be heavily loaded or directly decoupled. Refer to section 2.2.

1.3 Error Amplifier

The AS1012 error amplifier (pins 3, 4 and 5) is a high speed operational amplifier. This op amp is left totally uncommitted in order to accommodate a wide variety of control and loop compensation schemes. It has a gain/bandwidth product (GBW) of 5 MHz and can source up to 10 mA. Current sink capability is about 1 mA, and this can be increased by adding external DC loading.

The inputs of the error amplifier are an NPN differential pair. The input range is 1.2 to 3.8 volts. Each input is clamped to ground with a 5 volt Zener diode. The output of the error amplifier is an NPN emmitter follower with a fixed current source pulldown and an output range of 50 mV to 17 V. Refer to section 2.5 for information on using the error amplifier.

1.4 PWM Comparator

The AS1012 PWM (pulse-width modulator) comparator is a multi-input, high speed comparator that has a common mode range including ground as well as a very high AC common mode rejection. The pins associated with the PWM comparator are: RAMP (pin 11), SS (pin 13), and PWM (pin 15).

The PWM comparator generates the pulses that drive the output stage, which, in turn, drives the power switching device(s) of the power supply. An output pulse is initiated by the internal clock. The output stays high until the positive going ramp at the (+) input of the PWM comparator exceeds the lower of the three other inputs, at which point the output pulse is terminated. In this way, a variable duty cycle output is produced (Figure 16).

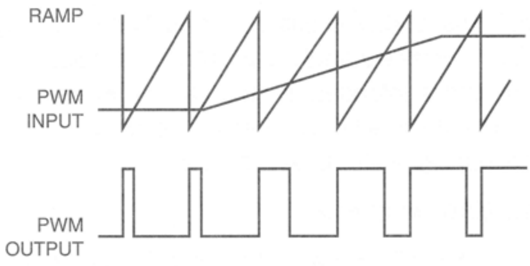


Figure 16. Pulse Width Modulation

The following paragraphs describe each input of the PWM comparator. Specific examples of voltage mode and current mode PWM arrangements are explained in section 2.3.

The RAMP input (+) is intended to be the reference of the PWM comparator and is usually connected to a ramp voltage waveform. For voltage mode control, this is usually the ramp waveform at CT (pin 13. For current mode control, the ramp waveform is normally derived from the switched primary current via a current sensing resistor or a current transformer. The ramp is compared to three other inputs, PWM, SS, and the oscillator trip point. Whenever the voltage at the RAMP input exceeds the voltage at the others, the output pulse is terminated.

PWM (–) is the control input of the PWM comparator and is normally connected to the output of the error amplifier. A varying level at PWM generates a varying duty cycle at the output (see Figure 16).

SS is the "soft start" input (–). This input is identical to the PWM input, except it has a built-in 60 μA current source so a grounded capacitor connected to this point creates a slow ramp, forcing a gradual rise in duty cycle at turn-on, but eventually rising to a level where it is out of the control loop. This capacitor is quickly discharged by an internal transistor during shutdown conditions. See sections 2.4. By clamping the SS pin to a level within the control range, a maximum duty cycle and/or power limit function can be implemented.

The final input to the PWM comparator is an internal oscillator input (–). This input is internally connected to the oscillator trip point and serves two functions. First, it blanks the output during discharge of CT to preclude 100% duty cycle. Second, it clamps the pulse width to nominal duration during Sync operation. Otherwise, as the ramp slope goes to zero, the loop gain would go to infinity.

Refer to section 2.3 for further discussions of the PWM comparator.

1.5 Current Limit Comparator

The current limit comparator of the AS1012 is a high speed, high-gain comparator with a wide common mode range including ground, a very high AC common mode rejection, and an accurate built-in offset of 1.25 volts. Both inputs are available (pins 16 and 17) and are fully differential, not relying on the integrity of a common ground between the sense elements and the IC. This, together with a –0.1 to 12 volt common mode range, allows cycle-by-cycle current limiting of either load or switch current. The output of the current limit comparator ties directly into the output logic. The nature of this design allows an extremely fast termination of the output pulse upon detection of an over current (when the CL(+) input is greater that 1.25 volts above the CL(–) input), with a typical propagation delay of only 125 ns. The current limit comparator can also be used for duty cycle clamping. Refer to section 2.6.

1.6 Output Stage

The OUTPUT stage of the AS1012 is a high current totem pole output designed to directly drive power MOSFET devices. The OUTPUT pin (pin 19 for SO package, pin 20 for DIP package) is normally connected directly to the gate drive circuitry. Included is an internal clamp that limits the output to 15 volts, protecting the FETs from excessive voltage when $V_{CC} > 15$ volts.

The DIP packaged devices offer separate output stage supply pins (V_C pin 1 and PWR GND pin 19). This is especially important as it allows separate decoupling and wiring of the drive circuitry to minimize effects of noise and interference caused by high switched currents associated with driving power devices. See section 2.7 for OUTPUT stage considerations.

1.7 Housekeeping Functions

The AS1012 has two additional functions. First, the programmable UVLO (under-voltage lockout pin 7) function, holds the IC in a low current "shutdown" mode until the voltage at this pin exceeds 2.5 volts. When in this mode, all PWM functions are shutdown, the reference at pin 6 is inhibited, the soft-start capacitor at pin 14 is discharged, and the output is clamped low. When the 2.5 volt threshold is exceeded, threshold voltage is shifted to a lower level (hysteresis) and the IC is allowed to turn on. The hysteresis allows bootstrapping or "burp starting." A simple voltage divider (usually tied to V_{CC}) is used to program the start-up/shutdown levels.

A second means of putting the IC in the shutdown mode is the Remote On/Off input (pin 8). This is a high impedance TTL level input that provides the same degree of shutdown as the UVLO function. A TTL low enables the IC while a TTL high (or floating) disables the IC. See section 2.8 for applications.

1.8 Over Temperature Protection

The AS1012 has another protective feature: built-in over temperature protection. The IC shuts down whenever the die temperature exceeds 115° C. The shutdown mode is the same as the UVLO and OFF functions. Hysteresis prevents the IC from toggling in and out of the shutdown mode. The IC restarts automatically once the temperature drops to a safe level.

SECTION 2 — CIRCUIT APPLICATION

Implementing the AS1012 in typical applications follows and expands upon the information presented in section 1. Refer to the functional block diagram.

2.1 Oscillator Set-Up

This section covers design guidelines for the three areas associated with the oscillator: 1) setting the frequency, which involves selection of RT and CT, 2) synchronizing the oscillator to an external frequency, and 3) implementing the feed-forward function.

2.1.1 Setting the Frequency

Setting the frequency of the AS1012 involves selecting the values of RT and CT. Figure 17 shows a graph relating the values of CT and frequency to RT. Although many different combinations of RT and CT give the same frequency, an optimum value for RT is 3.9 kΩ, as this value results in the best overall oscillator performance. To set the frequency of the AS1012, first choose a value of RT at or near 3.9 kΩ and then use the graph in Figure 3 to select the appropriate value of CT to give the desired frequency.

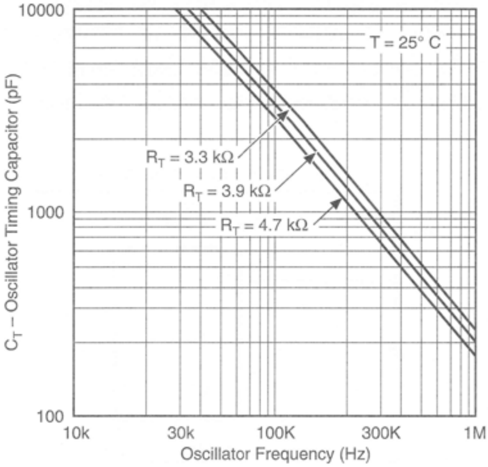


Figure 17. Optimum R_T vs C_T and Oscillator Frequency

2.1.2 Synchronizing the Oscillator

The first requirement for synchronizing the AS1012 to an external frequency is the oscillator be set to a frequency higher than the Sync frequency. This is done as described in section 2.1.1. Although any reasonable arbitrary waveform can be used, synchronization of the oscillator is best accomplished by applying a TTL level square wave (symmetrical) signal to the SYNC pin (Figure 16). The only requirement of an alternative to a square wave is that its positive (> 1.5 V) duration must be, at a minimum, equal to the duration of the discharge of CT plus a short delay (100 ns is usually sufficient). The Sync pulse must then go low (≤ 1.2 V) before the oscillator ramp reaches its upper threshold.

2.1.3 Implementing the Feed-Forward Function

As explained in section 1.1, the amplitude of the oscillator can be modulated via the FF pin to provide an open loop line regulation function. For current mode controlled converters, the feed-forward function normally inherent to the design since the primary current is proportional to the line voltage. Therefore, the oscillator's feed-forward function is typically used only in voltage mode controlled converters. Figure 18 shows that a simple divider off a line dependent rail is all that's required to implement the feedforward function.

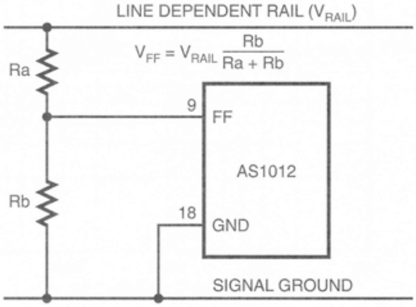

LINE DEPENDENT RAIL (V_{RAIL})
$V_{FF} = V_{RAIL} \frac{Rb}{Ra + Rb}$
Ra
Rb
9
FF
AS1012
18
GND
SIGNAL GROUND

Figure 18. Feed-Forward

Depending on which side (primary or secondary) the AS1012 is located, the line dependent rail can be either the bulk DC input voltage, an auxiliary winding voltage or the IC supply voltage, V_{CC}. The values of Ra and Rb are selected to give a $V_{FF} \geq$ 5 volts at low line. This gives a minimum ramp voltage of 3 volts. Avoid a ramp amplitude of less than three volts.

A simple way to select the divider values is to arbitrarily choose a relatively low value Rb, say 4.7 kΩ, to minimize any errors due to bias currents. Then use the relationship $V_{FF} = V_{RAIL}$ (Rb/Ra + Rb) to give V_{FF} = 5 V at low line.

2.2 V_{REF} Considerations

In most converters, Vref is normally connected directly to the error amplifier (+) input. In cases where it is used for other circuit functions, it may be necessary to decouple (filter) V_{REF}. Because of the nature of the V_{REF} circuitry, direct bypass with a capacitance of greater than 470 pF, without a series resistance of at least 100 Ω, must be avoided. In order to ensure good regulation, the current drain from V_{REF} should be limited to 5 mA or less.

2.3 PWM Comparator

The following describes employing the PWM comparator in the two most commonly used control methods—voltage mode control and current mode control.

2.3.1 Voltage Mode Control

Voltage mode control is defined as a system having a single control loop and regulates on the basis of the output voltage only (or some representation thereof). Figure 19 shows a typical voltage mode control scheme.

A duty cycle proportional to the output voltage is generated by the PWM comparator by comparing the amplified output divider voltage to the linear

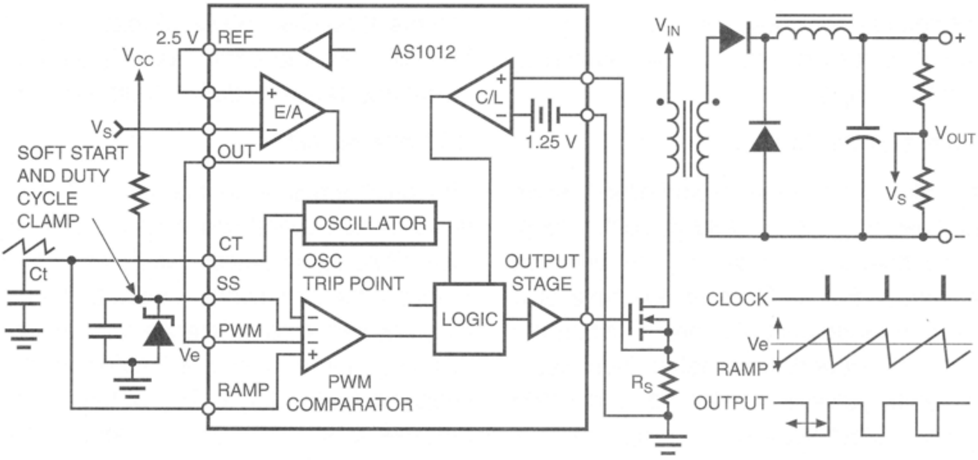


Figure 19. Voltage Mode Control

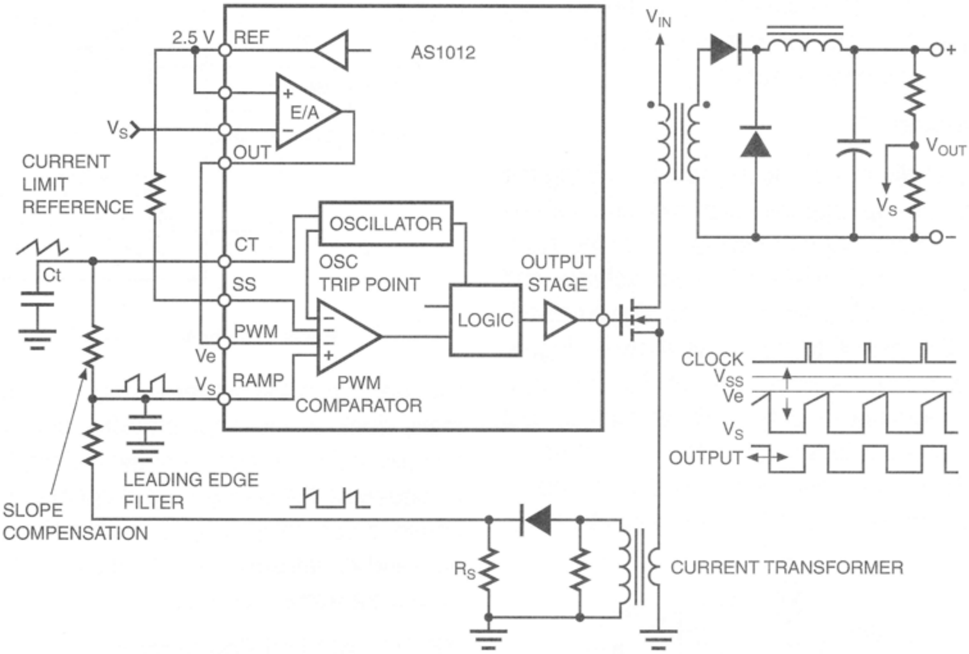


Figure 20. Current Mode Control

ramp waveform at CT (Figure 19). The output of the PWM comparator drives the output stage of the IC, which, in turn, drives the power switching devices of the supply.

2.3.2 Current Mode Control

Current mode control varies from voltage mode because, besides the outer voltage control loop, there is an inner loop monitoring the switched primary current. Figure 20 is an example of a typical current mode control scheme. When the primary current exceeds a predetermined value, the IC's output pulse is terminated. The PWM voltage (E/A output voltage) is compared to a voltage waveform derived from the switched primary current to generate a duty cycle proportional to both primary current and output voltage. A current sense resistor or current transformer monitors the primary current. In this example, V_{REF} is used as the current limit (or power limit) reference. A single resistor from CT to Ramp provides slope compensation.

2.4 Soft-Start

In many applications, it is necessary to bring the power supply up gradually to prevent instabilities or output overshoot that may occur during start-up. This is accomplished in both voltage and current mode converters by connecting a capacitor from SS (pin 14) to ground as shown in Figure 21. This creates a slow ramp at SS, forcing a gradual increase in duty cycle at turn-on, but eventually rising to a level where it is out of the control loop. The value of C_{SS} is determined by the relationship C = I(dt/dv). For example, if V_{SS} max. is 2.5 volts and we choose a soft-start time of 5 ms, then C_{SS} - 60 µA (5 ms/2.5 V) = 0.1 µF. The soft-start capacitor is quickly discharged by an internal transistor during shutdown conditions.

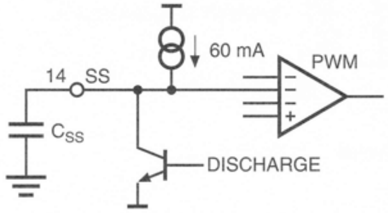


Figure 21. Soft-Start

2.5 Error Amplifier

The error amplifier in the AS1012 is a totally uncommitted operational amplifier allowing complete flexibility in power supply design. In most systems, the non-inverting input to the error amplifier is tied to a reference voltage while the inverting input monitors a fraction of the power supply output voltage. The output of the error amplifier is then the control input to the PWM comparator, which produces a varying duty cycle that is proportional to the supply output voltage. Figure 22 illustrates a typical hook-up of the error amplifier.

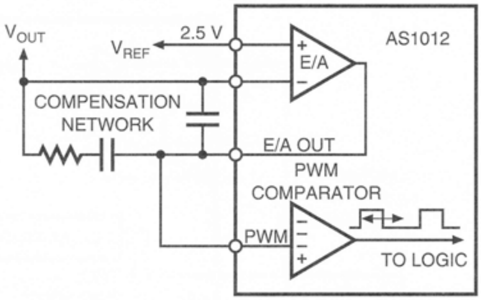


Figure 22. Error Amplifier Hook-Up

Compensating the power supply system is normally done at the error amplifier and a typical compensation network is shown. Compensation is required in the control loop to optimize the gain/phase characteristics of system. The network type and values are chosen to ensure stability and proper transient response.

2.6 Current Limit Comparator

The current limit comparator of the AS1012 can be used both as a current limit or duty cycle clamp. Figure 23 exemplifies how the current limit comparator is used to give cycle-by-cycle current

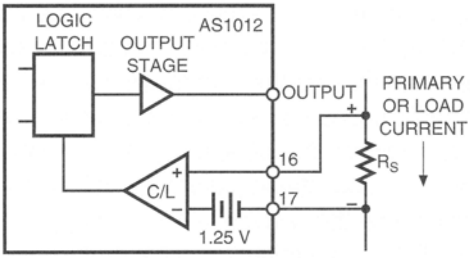


Figure 23. Current Limit

limiting. Whenever the current (primary, secondary or load) through the sense resistor causes a voltage of greater than 1.25 volts across Rs, the IC output pulse is terminated. Because of the 1.25 volt offset, it may be more practical to use a current transformer (Figure 20) to sense the current, as the power dissipation in the sense resistor becomes excessive for currents greater than 1 amp. This is the normal method of providing over current protection in voltage mode converters.

For duty cycle clamping in current mode converters (Figure 24), an RC off the IC output provides a voltage proportional to duty cycle at the C/L(+) input. A fixed level is applied to the C/L(–) input at the reference. As the duty cycle increases, the average voltage at C/L(+) also increases. Eventually it reaches the level at C/L(–), and the output pulse is terminated. In this way, the duty cycle can be clamped to any desirable value by adjusting the values of R and C and the reference voltage.

2.7 Remote On/Off

The AS1012 can be turned on and off remotely or by other circuitry (fault detection, timing, etc.) within the power supply by using the OFF pin as shown in Figure 27. The IC reverts to or remains in the shutdown mode whenever the OFF pin is allowed to go high. Any TTL level signal, open collector output, switch or relay contacts can be used to control the OFF pin. If remote On/Off is not required, simply ground the OFF pin locally to enable the IC.

2.8 Output Stage Considerations

The output stage of the AS1012 is capable of driving power MOSFET devices directly. The output clamps itself to a maximum of 15 volts to protect the FETs and to limit the transfer of energy to the gate capacitance beyond that required for switching (see Figure 26). Special care is required in the layout of the drive circuitry to minimize the effects of noise and interference caused by the high switched currents associated with driving power devices. For this reason, separate bypass and grounding is recommended for the output stage. The AS1012 DIP package has separate supply pins for the output stage (V_C and PWR GND), which further enhances the ability to control noise problems. For high power/high frequency designs, an external buffer stage is recommended in order to allow greater flexibility in layout (buffer can be located near the power devices) and to minimize the temperature rise of the IC. Figure 25 shows a typical FET drive circuit with the optional buffer arrangement.

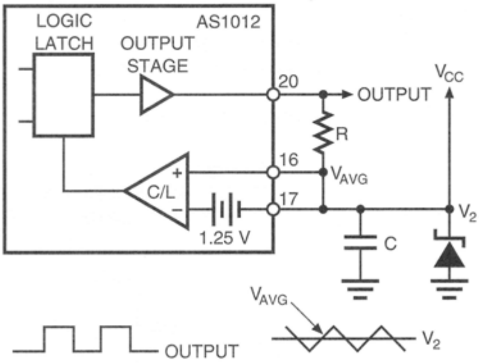


Figure 24. Cuty Cycle Clamp Using the C/L Comparator

2.9 UVLO (Under-Voltage Lockout)

The AS1012's programmable under-voltage lockout feature serves two important functions. First and foremost, it disables the IC until Vcc reaches a sufficient level to drive the FETs. Second, it provides a means to implement bootstrap and/or "burp" starting.

Figure 27 shows a simple resistor voltage divider is all that is required to program the UVLO. The value of R1 and R2 are selected so the voltage at UVLO is 2.5 volts when V_{CC} reaches the desired level of turn on — normally ≥ 10 volts. The values of R1 and R2 can be determined in a similar manner as those of the feed-forward divider. First, arbitrarily choose a relatively low resistance for R2 to minimize the effects of bias currents and noise. A good starting point for R2 is 10 kΩ. Second, use the relationship $R1 = (V_{CC\ ON} * R2/2.5) - R2$ to determine the value of R1.

For example:

> For a $V_{CC\ ON}$ of 10 V and an R2 of 10 kΩ, $R1 = (10*10{,}000/2.5) - 10{,}000 = 30$ kΩ.

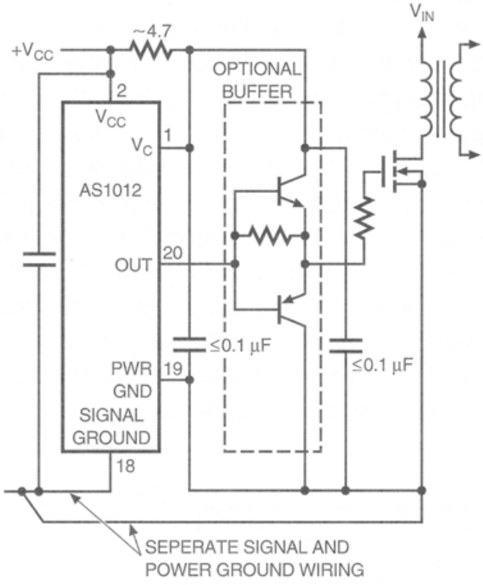


Figure 25. Output Stage

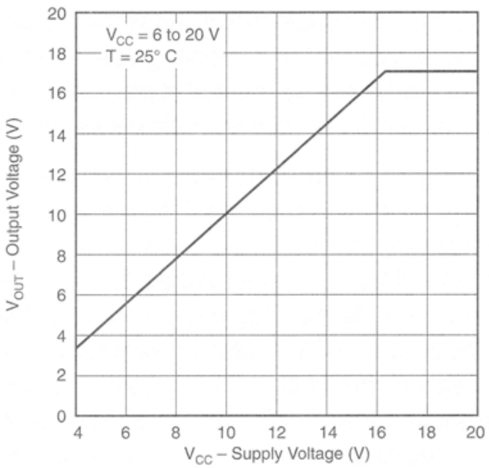


Figure 26. Internally Clamped Output Voltage vs Supply Voltage

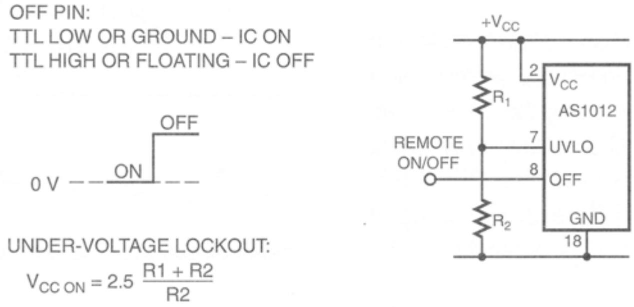
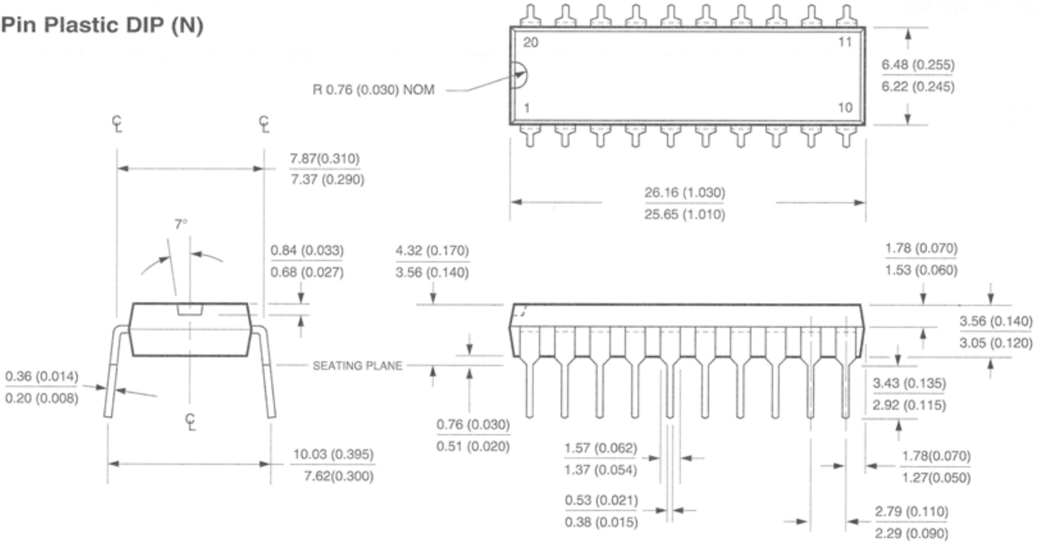


Figure 27. UVLO and Remote On/Off

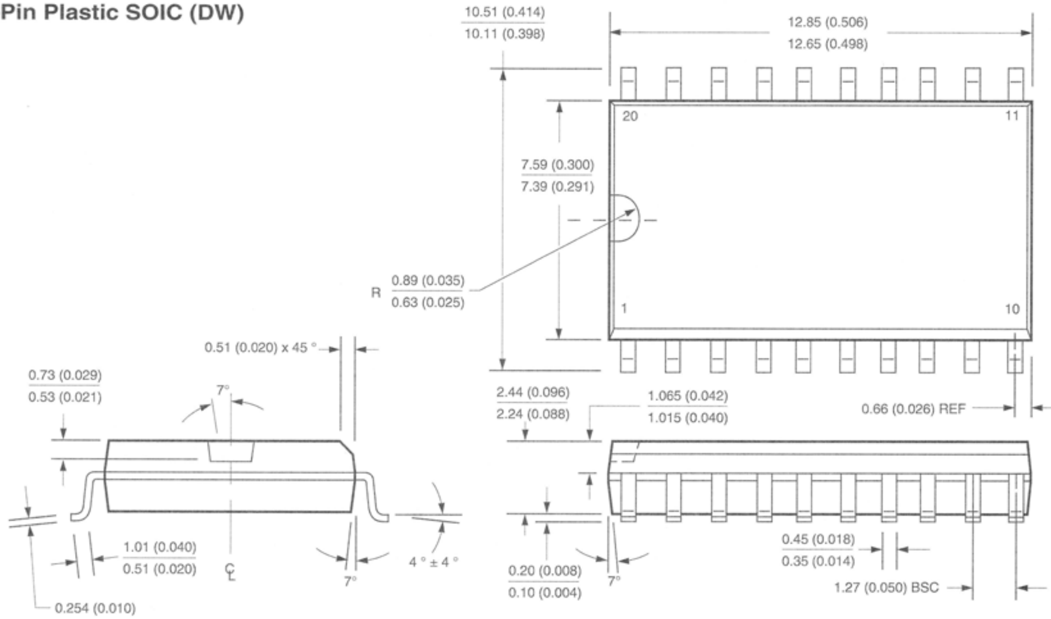
Package Dimensions

All Dimensions in mm (Inches)

20-Pin Plastic DIP (N)



20-Pin Plastic SOIC (DW)



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Notes

ASTEC

AS2842/3/4/5

Current Mode Controller

Preliminary Specification

Features

- 2.5 V bandgap reference trimmed to 0.5% and temperature-compensated
- Extended temperature range from - 40 to 105° C
- AS2842/3 oscillations trimmed for precision duty cycle clamp
- AS2844/5 have exact 50% max duty cycle clamp
- Advanced oscillator design simplifies synchronization
- Improved specs on UVLO and hysteresis provide more predictable start-up and shutdown
- Improved 5 V regulator provides better AC noise immunity
- Guaranteed performance with current sense pulled below ground
- Over-temperature shutdown

Description

The AS2842 family of control ICs provide pin-for-pin replacement of the industry standard UC3842 series of devices. The devices are redesigned to provide significantly improved tolerances in power supply manufacturing. The 2.5 V reference has been trimmed to 0.5% tolerance. The oscillator discharge current is trimmed to provide guaranteed duty cycle clamping rather than specified discharge current. The circuit is more completely specified to guarantee all parameters impacting power supply manufacturing tolerances.

In addition, the oscillator and flip-flop sections have been enhanced to provide additional performance. The R_T/C_T pin now doubles as a synchronization input that can be easily driven from open collector/open drain logic outputs. This sync input is a high impedance input and can easily be used for externally clocked systems. The new flip-flop topology allows the duty cycle on the AS2844/5 to be guaranteed between 49 and 50%. The AS2843/5 requires less than 0.5 mA of start-up current over the full temperature range.

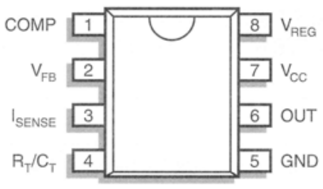
Ordering Information

Description	Temperature Range	Order Codes
8-Pin Plastic DIP	-40 to 105° C	AS2842/3/4/5N
8-Pin Plastic SOIC	-40 to 105° C	AS2842/3/4/5D-8
14-Pin Plastic SOIC	-40 to 105° C	AS2842/3/4/5D-14

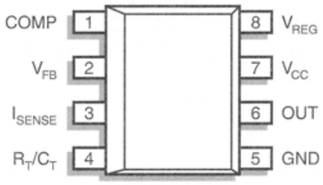
PRELIMINARY

Pin Configuration — Top view

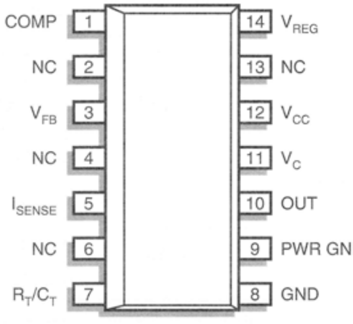
PDIP (N)



8L SOIC (D)



14L SOIC (D)



Functional Block Diagram

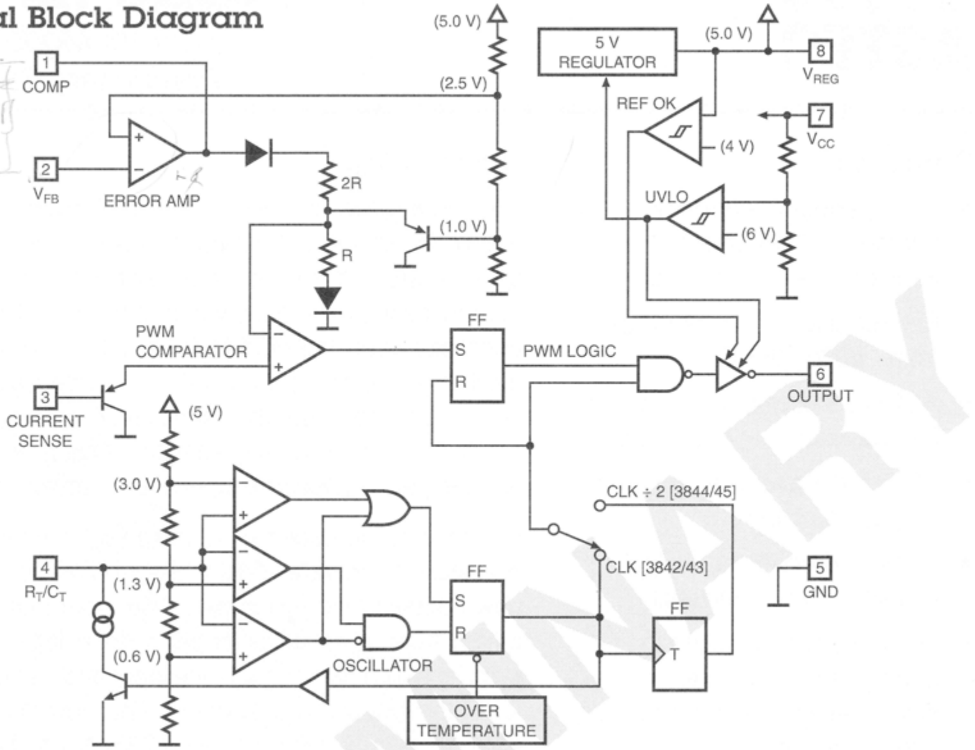


Figure 1. Block Diagram of the AS2842/3/4/5

PRELIMINARY

Pin Function Description

Pin Number	Function	Description
1	COMP	This pin is the error amplifier output. Typically used to provide loop compensation to maintain V_{FB} at 2.5 V.
2	V_{FB}	Inverting input of the error amplifier. The non-inverting input is a trimmed 2.5 V bandgap reference.
3	Current Sense	A voltage proportional to inductor current is connected to the input. The PWM uses this information to terminate the gate drive of the output.
4	R_T/C_T	Oscillator frequency and maximum output duty cycle are set by connecting a resistor (R_T) to V_{REG} and a capacitor (C_T) to ground. Pulling this pin to ground or to V_{REG} will accomplish a synchronization function.
5	GND	Circuit common ground, power ground, and IC substrate.
6	Output	This output is designed to directly drive a power MOSFET switch. This output can sink or source peak currents up to 1A. The output for the AS2844/5 switches at one-half the oscillator frequency.
7	V_{CC}	Positive supply voltage for the IC.
8	V_{REG}	This 5 V regulated output provides charging current for the capacitor C_T through the resistor R_T.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage ($I_{CC} < 30$ mA)	V_{CC}	Self-Limiting	V
Supply Voltage (Low Impedance Source)	V_{CC}	30	V
Output Current	I_{OUT}	±1	A
Output Energy (Capacitive Load)		5	μJ
Analog Inputs (Pin 2, Pin 3)		−0.3 to 30	V
Error Amp Sink Current		10	mA
Maximum Power Dissipation	P_D		
8L SOIC		750	mW
8L PDIP		1000	mW
14L SOIC		950	mW
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}		
AS2842,4		15	V
AS2843,5		10	V
Oscillator	f_{OSC}	50 to 500	kHz

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
8L PDIP	95° C/W	50° C/W	10.5 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C
14L SOIC	130° C/W	35° C/W	7.7 mW/°C

PRELIMINARY

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (-40 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5 V Regulator						
Output Voltage	V_{REG}	T_J = 25° C, I_{REG} = 1 mA	4.95	5.00	5.05	V
Line Regulation	PSRR	$12 \le V_{CC} \le 25$ V		2	10	mV
Load Regulation		$1 \le I_{REG} \le 20$ mA		2	10	mV
Temperature Stability[1]	TC_{REG}			0.2	0.4	mV/°C
Total Output Variation[1]		Line, load, temperature	4.85		5.15	V
Long-term Stability[1]		Over 1,000 hrs at 25° C		5	25	mV
Output Noise Voltage	V_{NOISE}	10 Hz $\le f \le$ 100 kHz, T_J = 25° C		50		µV
Short Circuit Current	I_{SC}		30	100	180	mA
2.5 V Internal Reference						
Nominal Voltage	V_{FB}	T = 25° C; I_{REG} = 1 mA	2.470	2.500	2.535	V
Line Regulation	PSRR	12 V $\le V_{CC} \le$ 25 V		2	5	mV
Load Regulation		$1 \le I_{REG} \le 20$ mA		2	5	mV
Temperature Stability[1]	TC_{VFB}			0.1	0.2	mV/°C
Total Output Variation[1]		Line, load, temperature	2.450	2.500	2.550	V
Long-term Stability[1]		Over 1,000 hrs at 125° C		2	12	mV
Oscillator						
Initial Accuracy	f_{OSC}	T_J = 25° C	47	52	57	kHz
Voltage Stability		12 V $\le V_{CC} \le$ 25 V		0.2	1	%
Temperature Stability[1]	TC_f	$T_{MIN} \le T_J \le T_{MAX}$		5		%
Amplitude	f_{OSC}	$V_{RT/CT}$ peak-to-peak		1.6		V
Upper Trip Point	V_H			2.9		V
Lower Trip Point	V_L			1.3		V
Sync Threshold	V_{SYNC}		400	600	800	mV
Discharge Current	I_D		7.5	8.7	9.5	mA
Duty Cycle Limit		R_T = 680 Ω, C_T = 5.3 nF, T_J = 25° C	46	50	52	%

PRELIMINARY

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (-40 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error Amplifier						
Input Voltage	V_{FB}	$T_J = 25°$ C	2.470	2.50	2.535	V
Input Bias Current	I_{BIAS}			−0.1	−1	μA
Voltage Gain	A_{VOL}	$2 \le V_{COMP} \le 4$ V	65	90	1	dB
Transconductance	G_m			1		mA/mV
Unity Gain Bandwidth[1]	GBW		0.8	1.2		MHz
Power Supply Rejection Ratio	PSRR	$12 \le V_{CC} \le 25$ V	60	70		dB
Output Sink Current	I_{COMPL}	V_{FB} = 2.7 V, V_{COMP} = 1.1V	2	6		mA
Output Source Current	I_{COMPH}	V_{FB} = 2.3 V, V_{COMP} = 5 V	0.5	0.8		mA
Output Swing High	V_{COMPH}	V_{FB} = 2.3 V, R_L = 15 kΩ to Ground	5	5.5		V
Output Swing Low	V_{COMPL}	V_{FB} = 2.7 V, R_L = 15 kΩ to Pin 8		0.7	1.1	V
Current Sense Comparator						
Transfer Gain[2,3]	AV_{CS}	$-0.2 \le V_{SENSE} \le 0.8$ V	2.85	3.0	3.15	V/V
I_{SENSE} Level Shift[2]	V_{LS}	V_{SENSE} = 0 V		1.5		V
Maximum Input Signal[2]		V_{COMP} = 5 V	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	$12 \le V_{CC} \le 25$ V		70		dB
Input Bias Current	I_{BIAS}			−1	−10	μA
Propagation Delay to Output[1]	t_{PD}			85	150	ns
Output						
Output Low Level	V_{OL} V_{OL}	I_{SINK} = 20 mA I_{SINK} = 200 mA		0.1 1.5	0.4 2.2	V V
Output High Level	V_{OH} V_{OH}	I_{SOURCE} = 20mA I_{SOURCE} = 200mA	13 12	13.5 13.5		V V
Rise Time[1]	t_R	C_L = 1 nF		50	150	ns
Fall Time[1]	t_F	C_L = 1 nF		50	150	ns
Housekeeping						
Start-up Threshold	V_{CC}(on)	3842/4 3843/5	15 7.8	16 8.4	17 9.0	V V
Minimum Operating Voltage After Turn On	V_{CC}(min)	3842/4 3843/5	9 7.0	10 7.6	11 8.2	V V
Output Low Level in UV State	V_{OUV}	I_{SINK} = 20 mA, V_{CC} = 6 V		1.5	2.0	V
Over-Temperature Shutdown[4]	T_{OT}			125		°C

PRELIMINARY

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (-40 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Duty Cycle	D_{max}	3842/3	94	97	100	%
Minimum Duty Cycle	D_{min}	3842/3			0	%
Maximum Duty Cycle	D_{max}	3844/5	49	49.5	50	%
Minimum Duty Cycle	D_{min}	3844/5			0	%
Start-up Current	I_{CC}	3842/4, $V_{FB} = V_{SENSE} = 0$ V, $V_{CC} = 14$ V		0.5	1.0	mA
		3843/5, $V_{FB} = V_{SENSE} = 0$ V, $V_{CC} = 7$ V		0.3	0.5	mA
Operating Supply Current	I_{CC}			9	17	mA
V_{CC} Zener Voltage	V_Z	I_{CC} = 25 mA		30		V

Notes:

1. This parameter is not 100% tested in production.
2. Parameter measured at trip point of PWM latch.
3. Transfer gain is the relationship between current sense input and corresponding error amplifier output at the PWM latch trip point and is mathematically expressed as follows:

$$A = \frac{\Delta I_{COMP}}{\Delta V_{SENSE}}; -0.2 \le \mathrm{V}_{\mathrm{SENSE}} \le 0.8\ V$$

4. At the over-temperature threshold, T_{OT}, the oscillator is disabled. The 5 V reference and the PWM stages, including the PWM latch, remain powered.

PRELIMINARY

Typical Performance Curves

PRELIMINARY

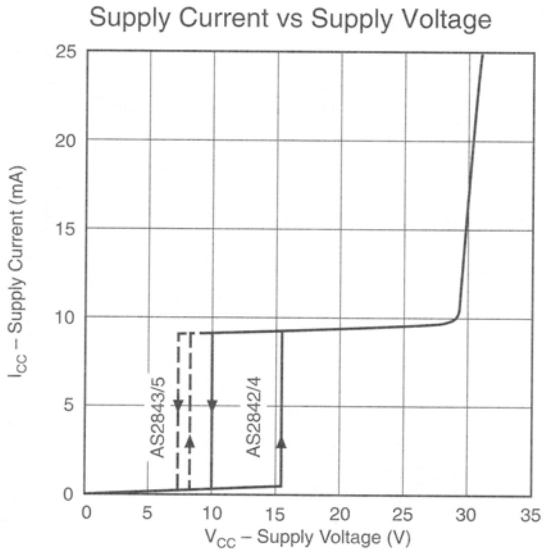


Figure 2

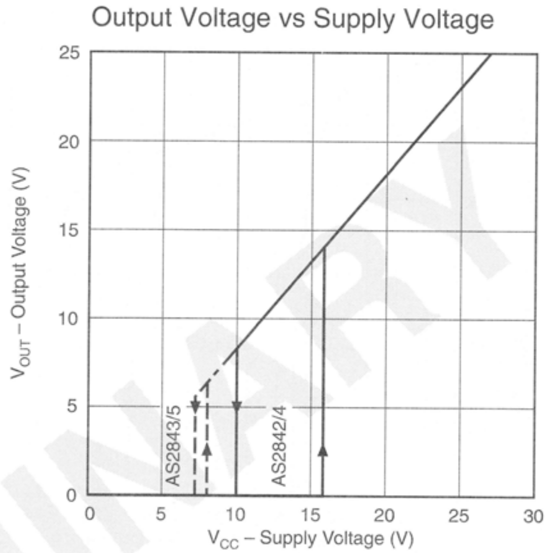


Figure 3

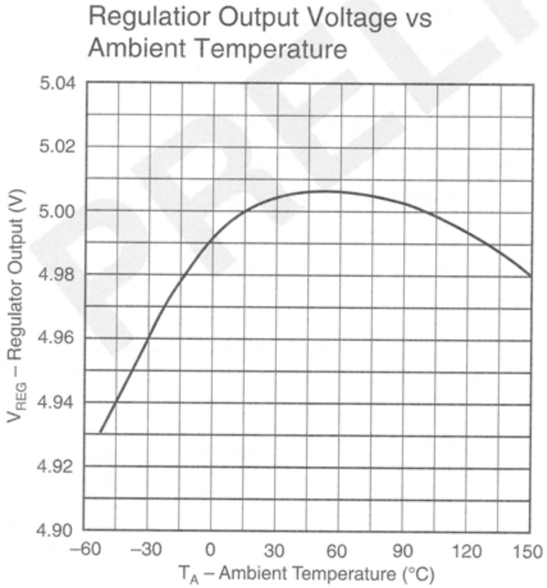


Figure 4

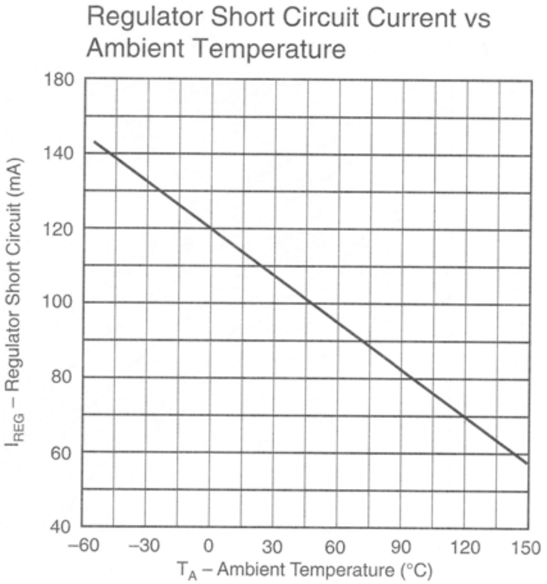


Figure 5

Typical Performance Curves

Regulator Load Regulation

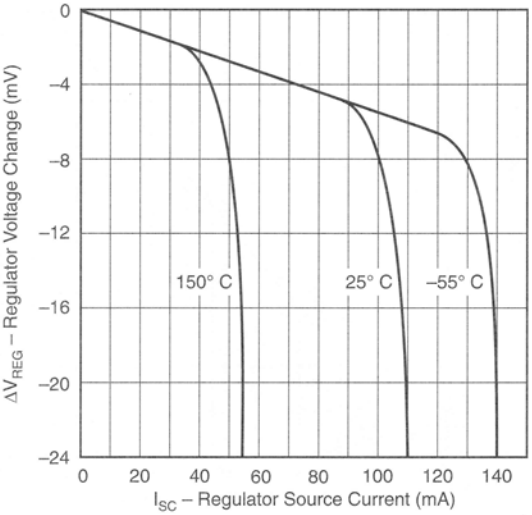


Figure 6

Maximum Duty Cycle vs Timing Resistor

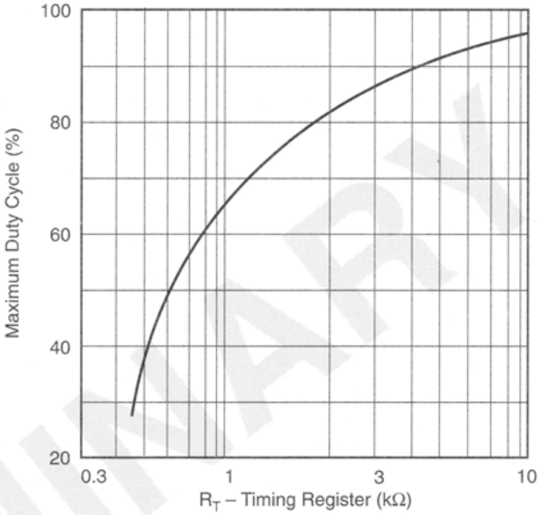


Figure 7

Timing Capacitor vs Oscillator Frequency

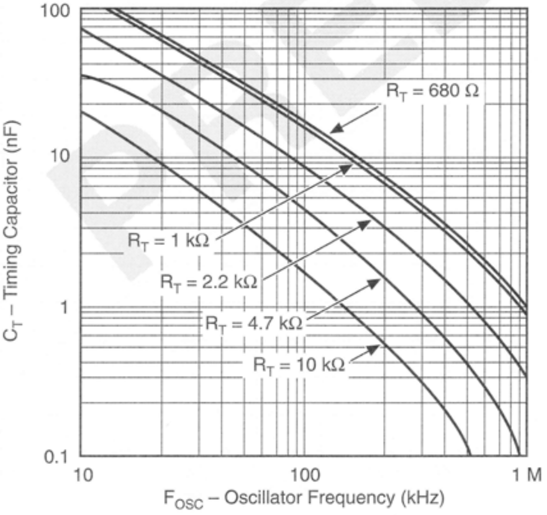


Figure 8

Maximum Duty Cycle Temperature Stability

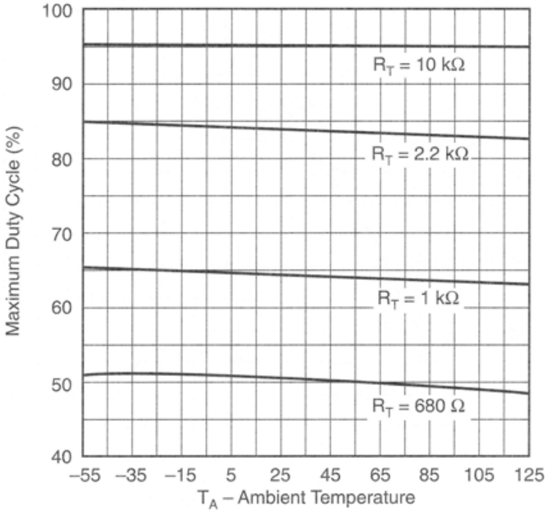


Figure 9

PRELIMINARY

Typical Performance Curves

Current Sense Input Threshold vs Error Amp Output Voltage

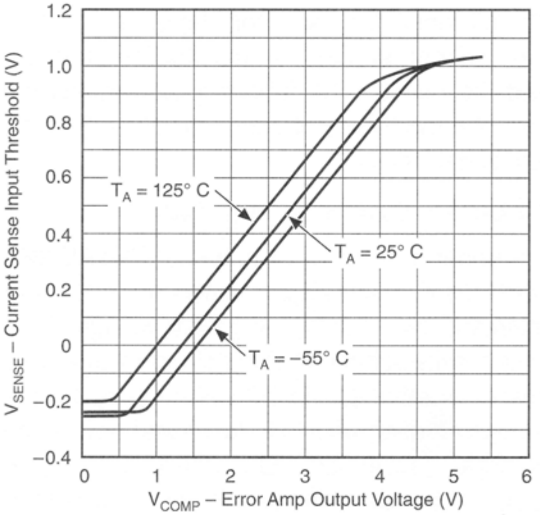


Figure 10

Error Amp Input Voltage vs Ambient Temperature

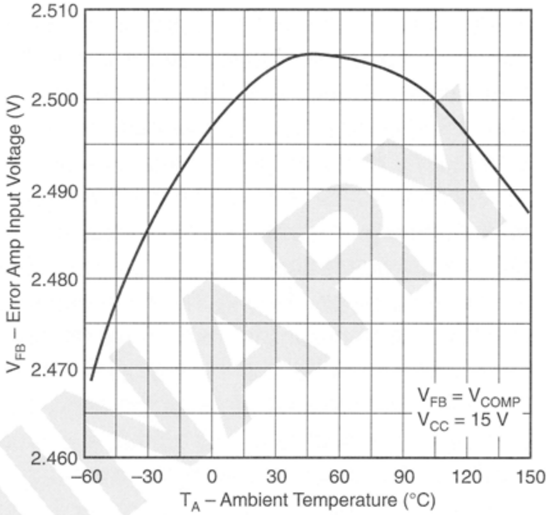


Figure 11

Output Sink Capability In Under-Voltage Mode

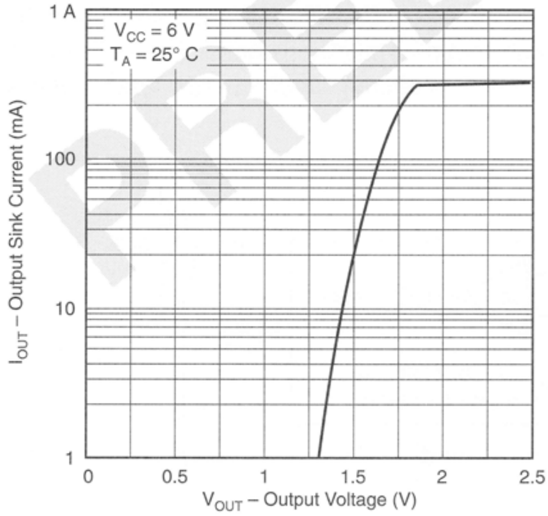


Figure 12

Output Saturation Voltage

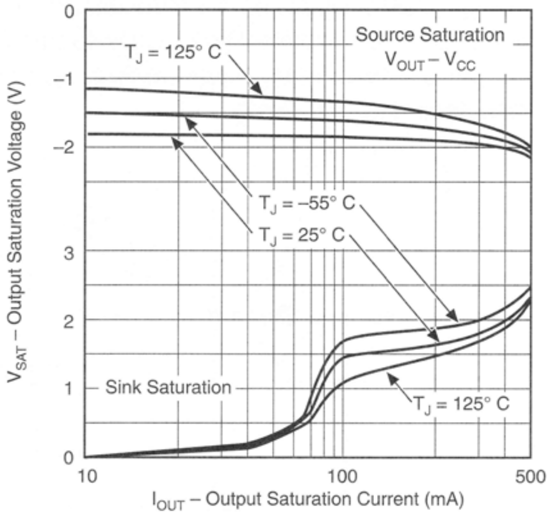


Figure 13

PRELIMINARY

Application Information

The AS2842/3/4/5 family of current-mode control ICs are low cost, high performance controllers which are pin compatible with the industry standard UC3842 series of devices. Suitable for many switch mode power supply applications, these ICs have been optimized for use in high frequency off-line and DC-DC converters. The AS2842 has been enhanced to provide significantly improved performance, resulting in exceptionally better tolerances in power supply manufacturing. In addition, all electrical characteristics are guaranteed over the full 0 to 105 °C temperature range. Among the many enhancements are: a precision trimmed 2.5 volt reference (±0.5% of nominal at the error amplifier input), a significantly reduced propagation delay from current sense input to the IC output, a trimmed oscillator for precise duty-cycle clamping, a modified flip-flop scheme that gives a true 50% duty ratio clamp on 3844/45 types, and an improved 5 V regulator for better AC noise immunity. Furthermore, the AS2842 provides guaranteed performance with current sense input below ground. The advanced oscillator design greatly simplifies synchronization. The device is more completely specified to guarantee all parameters that impact power supply manufacturing tolerances.

Section 1— Theory of Operation

The functional block diagram of the AS2842 is shown in Figure 01. The IC is comprised of the six basic functions necessary to implement current mode control; the under voltage lockout; the reference; the oscillator; the error amplifier; the current sense comparator/PWM latch; and the output. The following paragraphs will describe the theory of operation of each of the functional blocks.

1.1 Undervoltage lockout (UVLO)

The undervoltage lockout function of the AS2842 holds the IC in a low quiescent current (≤ 1 mA) "standby" mode until the supply voltage (V_{CC}) exceeds the upper UVLO threshold voltage. This guarantees that all of the IC's internal circuitry are properly biased and fully functional before the output stage is enabled. Once the IC turns on, the UVLO threshold shifts to a lower level (hysteresis) to prevent V_{CC} oscillations.

The low quiescent current standby mode of the AS2842 allows "bootstrapping"—a technique used in off-line converters to start the IC from the rectified AC line voltage initially, after which power to the IC is provided by an auxiliary winding off the power supply's main transformer. Figure 14 shows a typical bootstrap circuit where capacitor (C) is

PRELIMINARY

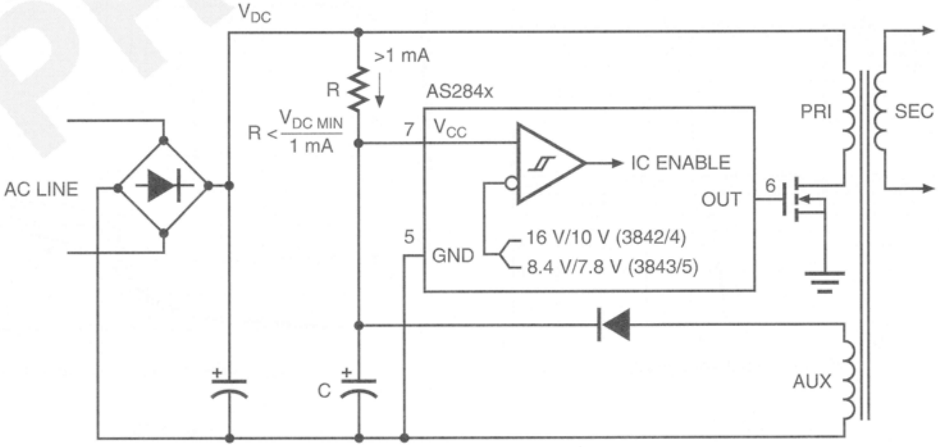


Figure 14. Boostrap Circuit

charged via resistor (R) from the rectified AC line. When the voltage on the capacitor (V_{CC}) reaches the upper UVLO threshold, the IC (and hence, the power supply) turns on and the voltage on C begins to quickly discharge due to the increased operating current. During this time, the auxiliary winding begins to supply the current necessary to run the IC. The capacitor must be sufficiently large to maintain a voltage greater than the lower UVLO threshold during start up. The value of R must be selected to provide greater than 1 mA of current at the minimum DC bus voltage (R < VDCmin/1 mA).

The UVLO feature of the AS2842 has significant advantages over standard 3842 devices. First, the UVLO thresholds are based on a temperature compensated band gap reference rather than conventional zeners. Second, the UVLO disables the output at power down, offering additional protection in cases where V_{REG} is heavily decoupled. The UVLO on some 3842 devices shuts down the 5 volt regulator only, which results in eventual power down of the output only after the 5 volt rail collapses. This can lead to unwanted stresses on the switching devices during power down. The AS2842 has two separate comparators which monitor both V_{CC} and V_{REF} and hold the output low if either are not within specification.

The AS2842 family offers two different UVLO options. The AS2842/4 has UVLO thresholds of 16 volts (on) and 10 volts (off). The AS2843/5 has UVLO levels of 8.4 volts (on) and 7.6 volts (off).

1.2 Reference (V_{REG} and V_{FB})

The AS2842 effectively has two precise band gap based temperature compensated voltage references. Most obvious is the V_{REG} pin (pin 8) which is the output of a series pass regulator. This 5.0 V output is normally used to provide charging current to the oscillator's timing capacitor (Section 1.3). In addition, there is a trimmed internal 2.5 V reference which is connected to the non-inverting (+) input of the error amplifier. The tolerance of the internal reference is ±0.5% over the full specified temperature range, and ±1% for V_{REG}.

The reference section of the AS2842 is greatly improved over the standard 3842 in a number of ways. For example, in a closed loop system, the voltage at the error amplifier's inverting input (V_{FB}, pin 1) is forced by the loop to match the voltage at the non-inverting input. Thus, V_{FB} is the voltage which sets the accuracy of the entire system. The 2.5 V reference of the AS2842 is tightly trimmed for precision at V_{FB}, including errors caused by the op amp, and is specified over temperature. This method of trim provides a precise reference voltage for the error amplifier while maintaining the original 5 V regulator specifications. In addition, force/sense (Kelvin) bonding to the package pin is utilized to further improve the 5 V load regulation. Standard 3842's, on the other hand, specify tight regulation for the 5 V output only and rate it over line, load and temperature. The voltage at V_{FB}, which is of critical importance, is loosely specified and only at 25° C.

The reference section, in addition to providing a precise DC reference voltage, also powers most of the IC's internal circuitry. Switching noise, therefore, can be internally coupled onto the reference. With this in mind, all of the logic within the AS2842 was designed with ECL type circuitry which generates less switching noise because it runs at essentially constant current regardless of logic state. This, together with improved AC noise rejection, results in substantially less switching noise on the 5 V output.

The reference output is short circuit protected and can safely deliver more than 20 mA to power external circuitry.

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1.3 Oscillator

The newly designed oscillator of the AS2842 is enhanced to give significantly improved performance. These enhancements are discussed in the following paragraphs. The basic operation of the oscillator is as follows:

A simple RC network is used to program the frequency and the maximum duty ratio of the AS2842 output. See Figure 15. Timing capacitor (C_T) is charged through timing resistor (R_T) from the fixed 5.0 V at V_{REG}. During the charging time, the OUT (pin 6) is high. Assuming that the output is not terminated by the PWM latch, when the voltage across C_T reaches the upper oscillator trip point (≈3.0 V), an internal current sink from pin 4 to ground is turned on and discharges C_T towards the lower trip point. During this discharge time, an internal clock pulse blanks the output to its low state. When the voltage across C_T reaches the lower trip point (≈1.3 V), the current sink is turned off, the output goes high, and the cycle repeats. Since the output is blanked during the discharge of C_T, it is the discharge time which controls the output deadtime and hence, the maximum duty ratio.

The nature of the AS2842 oscillator circuit is such that, for a given frequency, many combinations of R_T and C_T are possible. However, only one value of R_T will yield the desired maximum duty ratio at a given frequency. Since a precise maximum duty ratio clamp is critical for many power supply designs, the oscillator discharge current is trimmed in a unique manner which provides significantly improved tolerances as explained later in this section. In addition, the AS2844/5 options have an internal flip-flop which effectively blanks every other output pulse (the oscillator runs at twice the output frequency), providing an absolute maximum 50% duty ratio regardless of discharge time.

1.3.1 Selecting timing components R_T and C_T

The values of R_T and C_T can be determined mathematically by the following expressions:

$$C_T = \frac{D}{R_T f_{OSC} \ln\left(\frac{K_L}{K_H}\right)} = \frac{1.63D}{R_T f_{OSC}} \qquad (1)$$

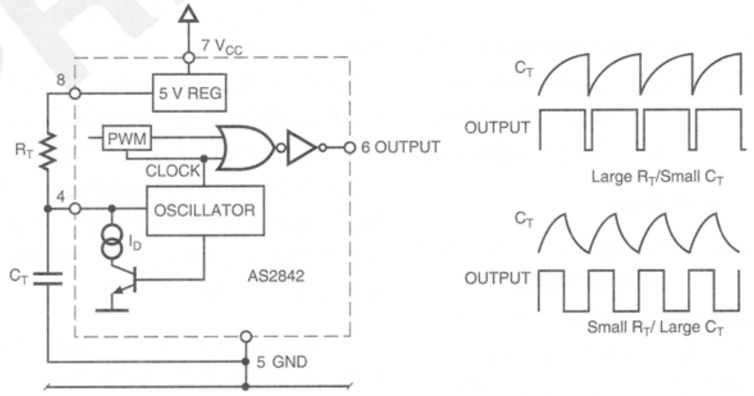

Figure 15. Osillator Set-up and Waveforms

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$$R_T = \frac{V_{REG}}{I_D} \cdot \frac{(K_L)^{\frac{1}{D}} - (K_H)^{\frac{1}{D}}}{(K_L)^{\frac{1-D}{D}} - (K_H)^{\frac{1-D}{D}}} \qquad (2)$$

$$= 582 \cdot \frac{(0.736)^{\frac{1}{D}} - (0.432)^{\frac{1}{D}}}{(0.736)^{\frac{1-D}{D}} - (0.432)^{\frac{1-D}{D}}}$$

$$\mathrm{K_L} = \frac{\mathrm{V_{REG}} - V_L}{V_{REG}} \approx 0.736 \qquad (3)$$

$$\mathrm{K_H} = \frac{\mathrm{V_{REG}} - V_H}{V_H} \approx 0.432 \qquad (4)$$

where f_{osc} is the oscillator frequency, D is the maximum duty ratio, V_H is the oscillator's upper trip point, V_L is the lower trip point, V_R is the Reference voltage, I_D is the discharge current.

Table 1 lists some common values of R_T and the corresponding maximum duty ratio. To select the timing components; first, use Table 1 or equation (2) to determine the value of R_T that will yield the desired maximum duty ratio. Then, use equation (1) to calculate the value of C_T. For example, for a switching frequency of 250 kHz and a maximum duty ratio of 50%, the value of R_T, from Table 1, is 683 Ω. Applying this value to equation (1) and solving for C_T gives a value of 4700 pF. In practice, some fine tuning of the initial values may be necessary during design. However, due to the advanced design of the AS2842 oscillator, once the final values are determined, they will yield repeatable results, thus eliminating the need for additional trimming of the timing components during manufacturing.

Table 1. R_T vs Maximum Duty Ratio

R_T (Ω)	Dmax
470	22%
560	37%
683	50%
750	54%
820	58%
910	63%
1,000	66%
1,200	72%
1,500	77%
1,800	81%
2,200	85%
2,700	88%
3,300	90%
3,900	91%
4,700	93%
5,600	94%
6,800	95%
8,200	96%
10,000	97%
18,000	98%

1.3.2 Oscillator enhancements

The AS2842 oscillator is trimmed to provide guaranteed duty ratio clamping. This means that the discharge current (I_D) is trimmed to a value that compensates for all of the tolerances within the device (such as the tolerances of V_{REG}, propagation delays, the oscillator trip points, etc.) which have an effect on the frequency and maximum duty ratio. For example, if the combined tolerances of a particular device are 0.5% above nominal, then I_D is trimmed to 0.5% above nominal. This method of trimming virtually eliminates the need to trim external oscillator components during power supply manufactur-

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ing. Standard 3842 devices specify or trim only for a specific value of discharge current. This makes precise and repeatable duty ratio clamping virtually impossible due to other IC tolerances. The AS2844/5 provides true 50% duty ratio clamping by virtue of excluding from its flip-flop scheme, the normal output blanking associated with the discharge of C_T. Standard AS2844/5 devices include the output blanking associated with the discharge of C_T, resulting in somewhat less than a 50% duty ratio.

1.3.3 Synchronization

The advanced design of the AS2842 oscillator simplifies synchronizing the frequency of two or more devices to each other or to an external clock. The R_T/C_T doubles as a synchronization input which can easily be driven from any open collector logic output. Figure 16 shows some simple circuits for implementing synchronization.

1.4 Error amplifier (COMP)

The AS2842 error amplifier is a wide bandwidth, internally compensated operational amplifier which provides a high DC open loop gain (90 dB). The input to the amplifier is a PNP differential pair. The non-inverting (+) input is internally connected to the 2.5 V reference, and the inverting (–) input is available at pin 2 (V_{FB}). The output of the error amplifier consists of an active pull-down and a 0.8 mA current source pull-up as shown in Figure 17. This type of output stage allows easy implementation of soft start, latched shutdown and reduced current sense clamp functions. It also permits wire "OR-ing" of the error amplifier outputs of several 3842s, or complete bypass of the error amplifier when its output is forced to remain in its "pull-up" condition.

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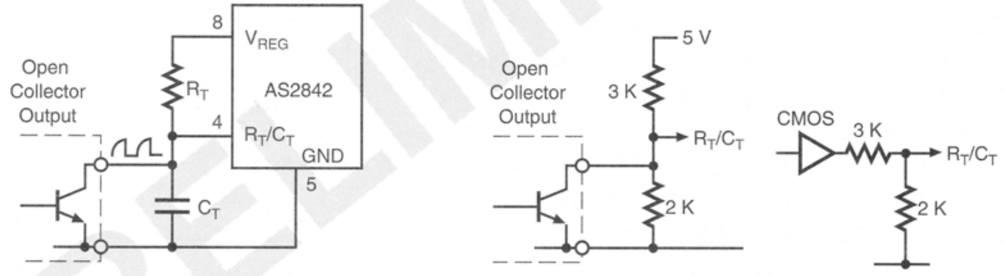

SYNC

EXTERNAL CLOCK

Figure 16. Synchronization

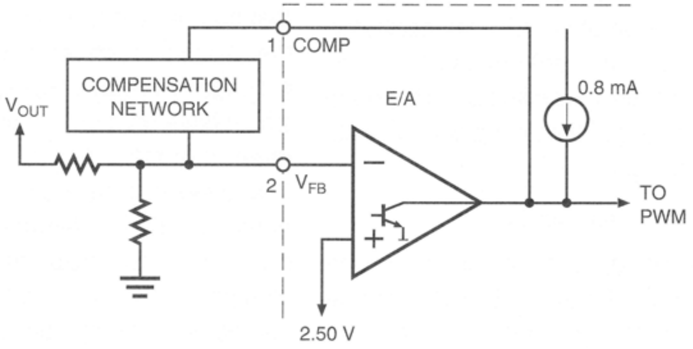

Figure 17. Error Amplifier Compensation

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In most typical power supply designs, the converter's output voltage is divided down and monitored at the error amplifier's inverting input, V_{FB}. A simple resistor divider network is used and is scaled such that the voltage at V_{FB} is 2.5 V when the converter's output is at the desired voltage. The voltage at V_{FB} is then compared to the internal 2.5 V reference and any slight difference is amplified by the high gain of the error amplifier. The resulting error amplifier output is level shifted by two diode drops and is then divided by three to provide a 0 to 1 V reference (V_E) to one input of the current sense comparator. The level shifting reduces the input voltage range of the current sense input and prevents the output from going high when the error amplifier output is forced to its low state. An internal clamp limits V_E to 1.0 V. The purpose of the clamp is discussed in Section 1.5.

1.4.1 Loop compensation

Loop compensation of a power supply is necessary to ensure stability and provide good line/load regulation and dynamic response. It is normally provided by a compensation network connected between the error amplifier's output (COMP) and inverting input as shown in Figure 17. The type of network used depends on the converter topology and in particular, the characteristics of the major functional blocks within the supply - i.e. the error amplifier, the modulator/switching circuit, and the output filter. In general, the network is designed such that the converters overall gain/phase response approaches that of a single pole with a –20 dB/decade rolloff, crossing unity gain at the highest possible frequency (up to $f_{SW}/4$) for good dynamic response, with adequate phase margin (> 45°) to ensure stability.

Figure 18 shows the Gain/Phase response of the error amplifier. The unity gain crossing is at 1.2 MHz with approximately 57° C of phase margin. This information is useful in determining the configuration and characteristics required for the compensation network.

One of the simplest types of compensation networks is shown in Figure 19. An RC network provides a single pole which is normally set to compensate for the zero introduced by the the output capacitor's ESR. The frequency of the pole (f_P) is determined by the formula;

$$f_P = \frac{1}{2\pi R_f C_f} \tag{5}$$

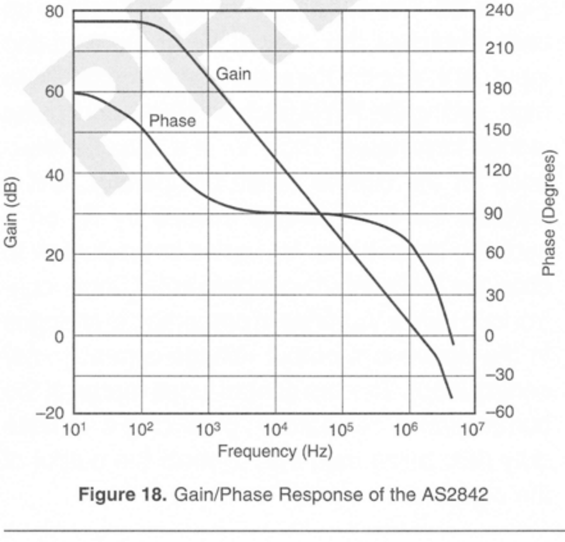

Figure 18. Gain/Phase Response of the AS2842

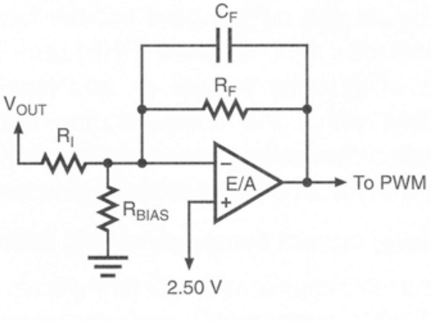

Figure 19. A Typical Compensation Network

Resistors R_1 and R_F set the low frequency gain and should be chosen to provide the highest possible gain, without exceeding the unity gain crossing frequency limit of $f_{SW}/4$. R_{BIAS}, in conjunction with R_1, sets the converter's output voltage; but has no effect on the loop gain/phase response.

There are a few converter design considerations associated with the error amplifier. First, the values of the divider network (R_1 and R_{BIAS}) should be kept low in order to minimize errors caused by the error amplifier's input bias current ($\approx -3.0\ \mu A$). An output voltage error equal to the product of the input bias current and the equivalent divider resistance, can be quite significant with divider values greater than 5 kΩ. Low divider resistor values also help to improve the noise immunity of the sensitive V_{FB} input.

The second consideration is that the error amplifier will typically source only 0.8 mA; thus, the value of feedback resistance (R_F) should be no lower than 5 kΩ in order to maintain the error amplifier's full output range. In practice, however, the feedback resistance required is usually much greater than 5 kΩ, hence this limitation is normally not a problem.

Some power supply topologies may require a more elaborate compensation network. For example, flyback and boost converters operating with continuous current have transfer functions that include a right half plane (RHP) zero. These types of systems require an additional pole element within the compensation network. A detailed discussion of loop compensation, however, is beyond the scope of this application note.

1.5 I_{SENSE} current comparator/PWM latch

The current sense comparator (sometimes called the PWM comparator) and accompanying latch circuitry make up the pulse width modulator (PWM). It provides pulse-by-pulse current sensing/limiting and generates a variable duty ratio pulse train which controls the output voltage of the power supply. Included is a high speed comparator followed by ECL type logic circuitry which has very low propagation delays and switching noise. This is essential for high frequency power supply designs. The comparator has been designed to provide guaranteed performance with the current sense input below ground. The PWM latch ensures that only one pulse is allowed at the output for each oscillator period.

The inverting input to the current sense comparator is internally connected to the level shifted output of the error amplifier (V_E) as discused in the previous section. The non-inverting input is the I_{SENSE} input (pin 3). It monitors the switched inductor current of the converter.

Figure 20 shows the current sense/PWM circuitry of the AS2842, and associated waveforms. The output is set high by an internal clock pulse and remains high until one of two conditions occur; 1) the oscillator times out (Section 1.3 or 2) the PWM latch is set by the current sense comparator. During the time when the output is high, the converter's switching device is turned on and current flows through resistor R_S. This produces a stepped ramp waveform at pin 3 as shown in Figure 20. The current will continue to ramp up until it reaches the level of V_E at the inverting input. At that point, the comparator's output goes high, setting the PWM latch and the output pulse is then terminated. Thus, V_E is a variable reference for the current sense comparator, and it controls the peak current sensed by R_S on a cycle-by-cycle basis. V_S varies in proportion to changes in the input voltage/current (inner control loop) while V_E varies in proportion to changes in the converters output voltage/current (outer control loop). The two control loops merge at the current sense comparator, producing a variable duty ratio pulse train that controls the output of the converter.

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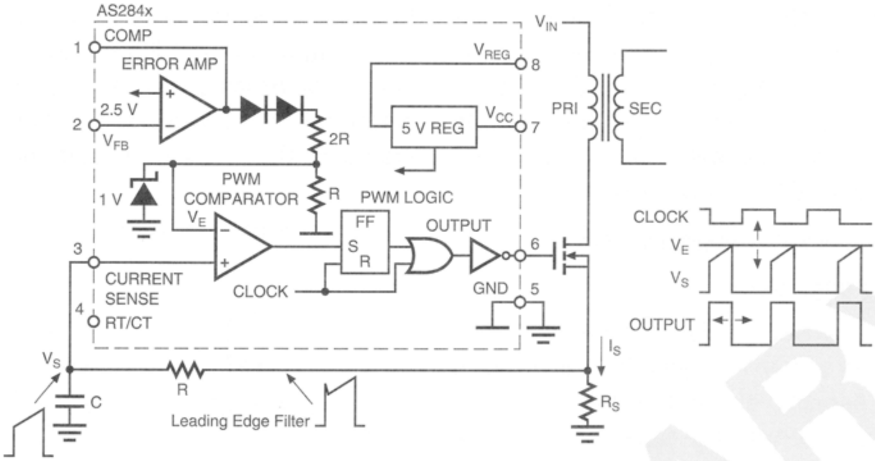

Figure 20. Current Sense/PWN Latch Circuit and Waveforms

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The current sense comparator's inverting input is internally clamped to a level of 1.0 V to provide a current limit (or power limit for multiple output supplies) function. The value of R_S is selected to produce 1.0 V at the maximum allowed current. For example, if 1.5 A is the maximum allowed peak inductor current, then R_S is selected to equal 1 V/1.5 A = 0.66 Ω. In high power applications, power dissipation in the current sense resistor may become intolerable. In such a case, a current transformer can be used to step down the current seen by the sense resistor. See Figure 21.

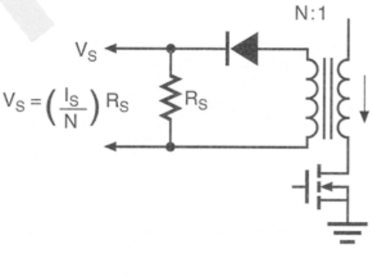

Figure 21. Optional Current Transformer

1.6 Output (OUT)

The output stage of the AS2842 is a high current totem-pole configuration that is well suited for directly driving power MOSFETs. It is capable of sourcing and sinking up to 1 A of peak current. Cross conduction losses in the output stage have been minimized resulting in lower power dissipation in the device. This is particularly important for high frequency operation. During undervoltage shutdown conditions, the output is active low. This eliminates the need for an external pulldown resistor.

1.7 Over-temperature shutdown

The AS2842 has a built-in over-temperature shutdown which will limit the die temperature to 130° C typically. When the over-temperature condition is reached, the oscillator is disabled. All other circuit blocks remain operational. Therefore, when the oscillator stops running, output pulses terminate without losing control of the supply or losing any peripheral functions that may be running off the 5 V regulator. The output may go high during the final cycle, but the PWM

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latch is still fully operative, and the normal termination of this cycle by the current sense comparator will latch the output low until the over-temperature condition is rectified. Cycling the power will reset the over-temperature disable mechanism, or the chip will re-start after cooling through a nominal hysteresis band.

Section 2 – Design Considerations

2.1 Leading edge filter

The current sensed by R_S contains a leading edge spike as shown in Figure 20. This spike is caused by parasitic elements within the circuit including the interwinding capacitance of the power transformer and the recovery characteristics of the rectifier diode(s). The spike, if not properly filtered, can cause stability problems by prematurely terminating the output pulse.

A simple RC filter is used to suppress the spike. The time constant should be chosen such that it approximately equals the duration of the spike. A good choice for R_1 is 1 kΩ, as this value is optimum for the filter and at the same time, it simplifies the determination of R_{SLOPE} (Section 2.2). If the duration of the spike is, for example, 100 ns, then C is determined by:

$$\begin{aligned} C &= \frac{\text{Time Constant}}{1\ \text{k}\Omega} \qquad (6) \\ &= \frac{100\ \text{ns}}{1\ \text{k}\Omega} \\ &= 100\ \text{pF} \end{aligned}$$

2.2 Slope compensation

Current-mode controlled converters can experience instabilities or subharmonic oscillations when operated at duty ratios greater than 50%. Two different phenomena can occur as shown

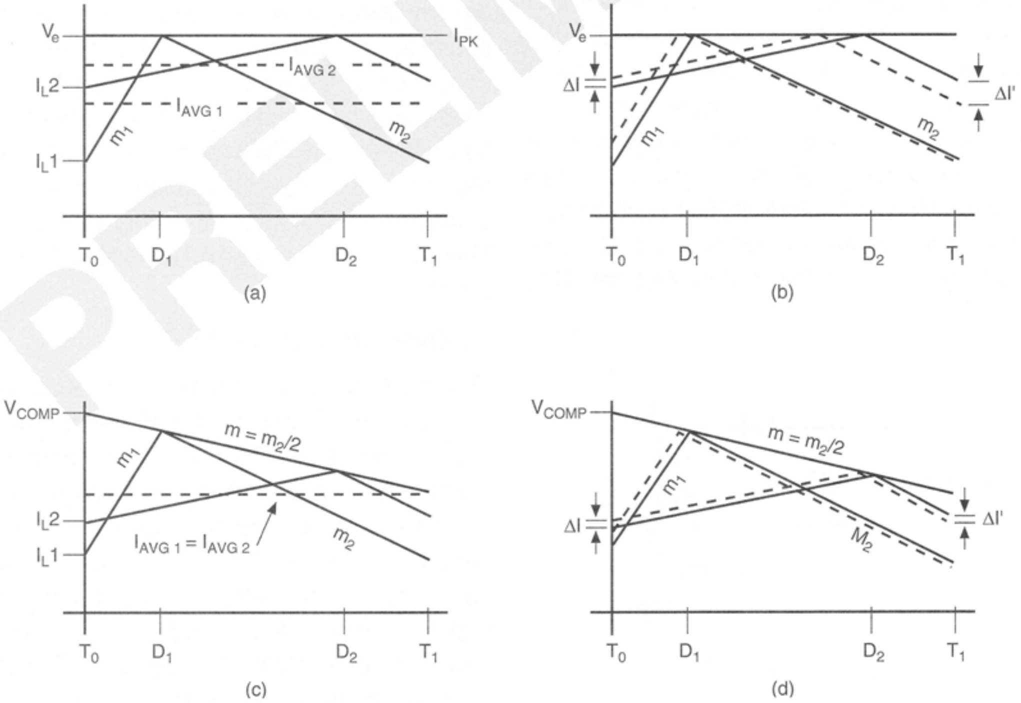

Figure 22. Slope Compensation

graphically in Figure 22.

First, current-mode controllers detect and control the peak inductor current, where as the converter's output corresponds to the average inductor current. Figure 22(a) clearly shows that the average inductor current (I_1 & I_2) changes as the duty ratio (D_1 & D_2) changes. Note that for a fixed control voltage, the peak current is the same for any duty ratio. The difference between the peak and average currents represents an error which causes the converter to deviate from true current-mode control.

Second, Figure 22(b) depicts how a small perturbation of the inductor current (ΔI) can result in an unstable condition. For duty ratios less than 50 %, the disturbance will quickly converge to a steady state condition. For duty ratios greater than 50 %, ΔI progressively increases on each cycle, causing an unstable condition.

Both of these problems are corrected simultaneously by injecting a compensating ramp into either the control voltage (V_E) as shown in Figure 22(c) & (d), or to the current sense waveform at pin 3. Since V_E is not directly accessible, and, a positive ramp waveform is readily available from the oscillator at pin 4, it is more practical to add the slope compensation to the current waveform. This can be implemented quite simply with the addition of a single resistor, R_{SLOPE}, between pin 4 and pin 3 as shown in Figure 23(a). R_{SLOPE}, in conjunction with the leading edge filter resistor, R_1 (Section 2.1), forms a divider network which determines the amount of slope added to the waveform. The amount of slope added to the current waveform is inversely proportional to the value of R_{SLOPE}. It has been determined that the amount of slope (m) required is equal to or greater than 1/2 the downslope (m_2) of the inductor current. Mathematically stated:

$$m \geq \frac{m_2}{2} \tag{7}$$

In some cases the required value of R_{SLOPE} may be low enough to affect the oscillator circuit and thus cause the frequency to shift. An emitter follower circuit can be used as a buffer for R_{SLOPE} as depicted in Figure 23(b).

Slope compensation can also be used to improve noise immunity in current mode converters operating at less than 50% duty ratio. Power supplies

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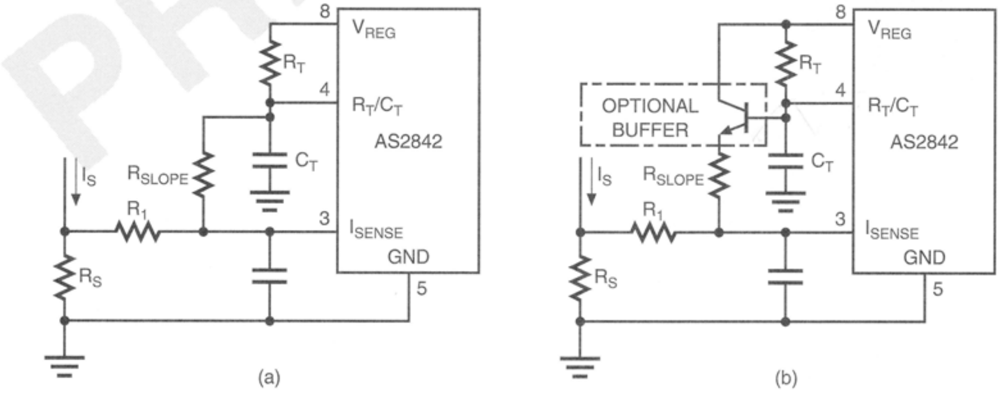

(a)

(b)

Figure 23. Slope Compensation

operating under very light load can experience instabilities caused by the low amplitude of the current sense ramp waveform. In such a case, any noise on the waveform can be sufficient to trip the comparator resulting in random and premature pulse termination. The addition of a small amount of artificial ramp (slope compensation) can eliminate such problems without drastically affecting the overall performance of the system.

2.3 Circuit layout and other considerations

The eletronic noise generated by any switch-mode power supply can cause severe stability problems if the circuit is not layed-out (wired) properly. A few simple layout practices will help to minimize noise problems.

When building prototype breadboards, never use plug-in protoboards or wire wrap construction. For best results, do all breadboarding on double sided PCB using ground plane techniques. Keep all traces and lead lengths to a minimum. Avoid large loops and keep the area enclosed within any loops to a minimum. Use common point grounding techniques and separate the power ground traces from the signal ground traces. Locate the control IC and circuitry away from switching devices and magnetics. Also, the timing capacitor's ground connection must be right at pin 5 as shown in Figure 15. These grounding and wiring techniques are very important because the resistance and inductance of the traces are significant enough to generate noise glitches which can disrupt the normal operation of the IC.

Also, to provide a low impedance path for high frequency noise, V_{CC} and V_{REF} should be decoupled to IC ground with 0.1 μF capacitors. Additional decoupling in other sensitive areas may also be necessary. It is very important to locate the decoupling capacitors as close as possible to the circuit being decoupled.

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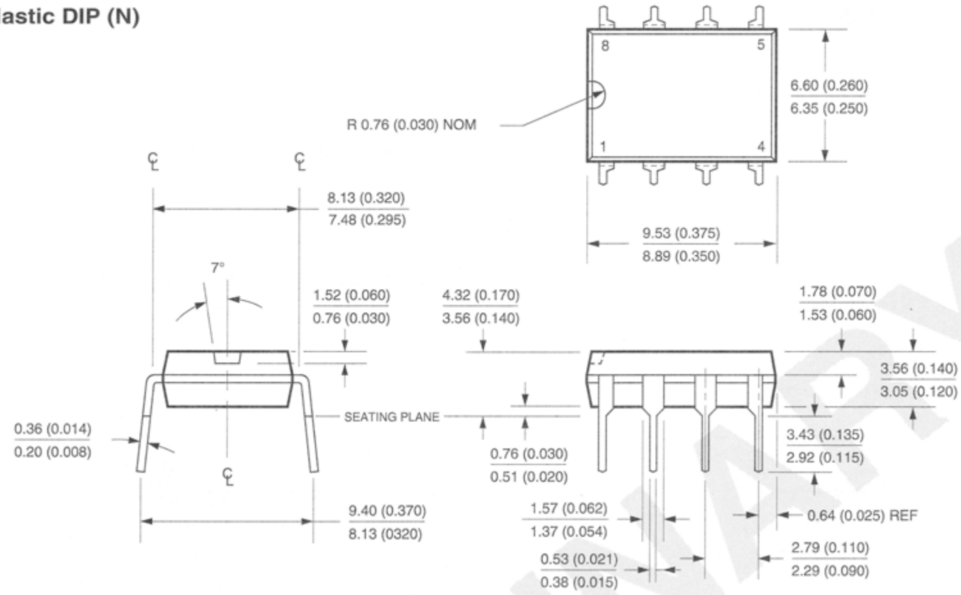
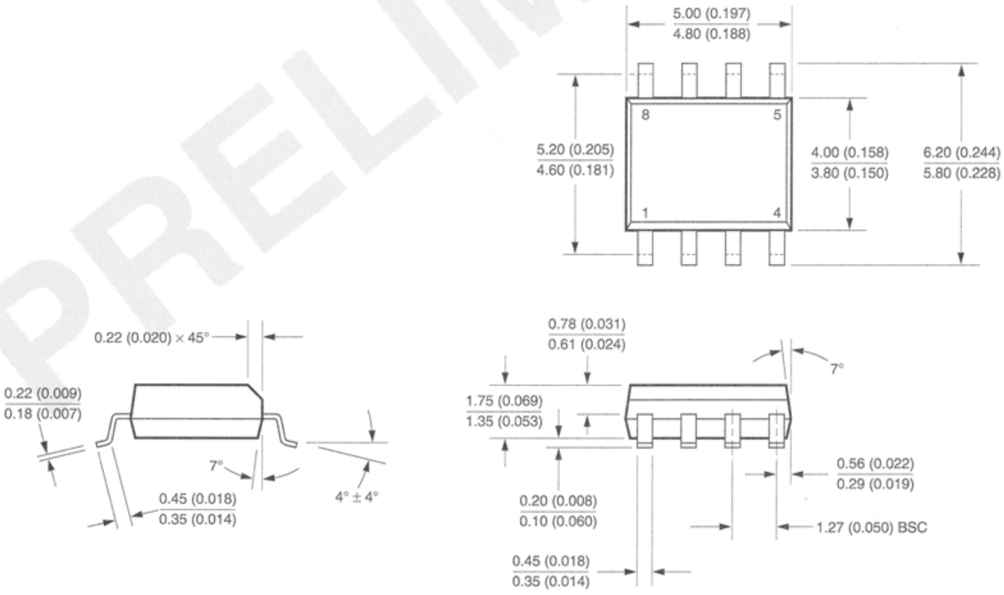
Package Dimensions

All Dimensions in mm (Inches)

8-Pin Plastic DIP (N)



8-Pin Plastic SOIC (D)

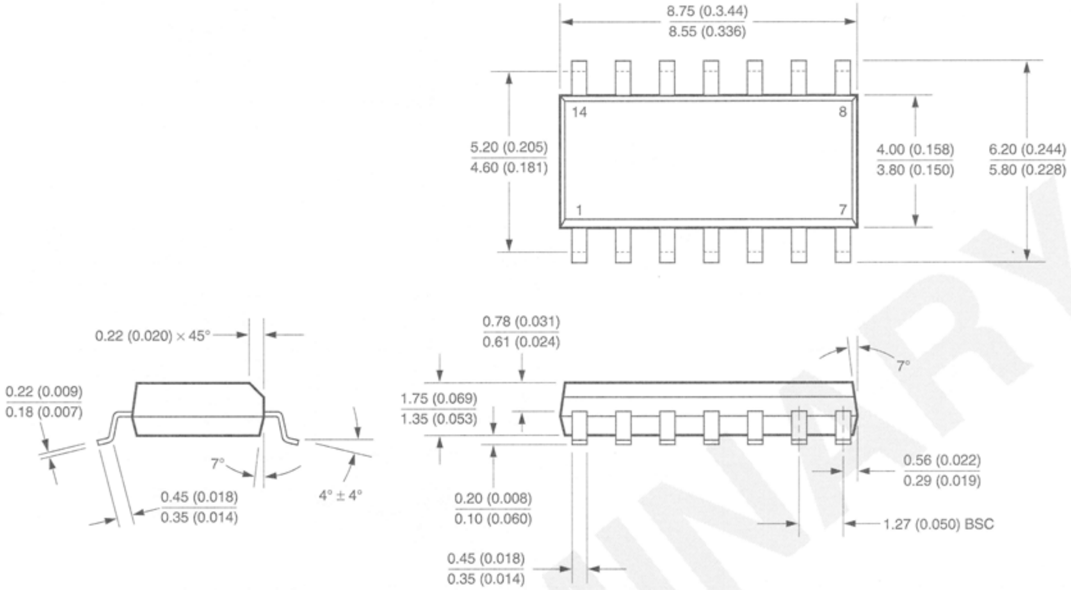


PRELIMINARY

Package Dimensions

All Dimensions in mm (Inches)

14-Pin Plastic SOIC (D)



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ASTEC

AS3842/3/4/5

Current Mode Controller

Features

- 2.5 V bandgap reference trimmed to 0.5% and temperature-compensated
- Standard temperature range extended to 105° C
- AS3842/3 oscillations trimmed for precision duty cycle clamp
- AS3844/5 have exact 50% max duty cycle clamp
- Advanced oscillator design simplifies synchronization
- Improved specs on UVLO and hysteresis provide more predictable start-up and shutdown
- Improved 5 V regulator provides better AC noise immunity
- Guaranteed performance with current sense pulled below ground
- Over-temperature shutdown

Description

The AS3842 family of control ICs provide pin-for-pin replacement of the industry standard UC3842 series of devices. The devices are redesigned to provide significantly improved tolerances in power supply manufacturing. The 2.5 V reference has been trimmed to 0.5% tolerance. The oscillator discharge current is trimmed to provide guaranteed duty cycle clamping rather than specified discharge current. The circuit is more completely specified to guarantee all parameters impacting power supply manufacturing tolerances.

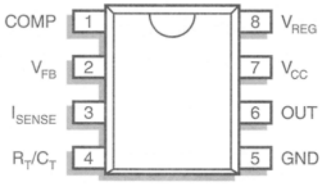
In addition, the oscillator and flip-flop sections have been enhanced to provide additional performance. The R_T/C_T pin now doubles as a synchronization input that can be easily driven from open collector/open drain logic outputs. This sync input is a high impedance input and can easily be used for externally clocked systems. The new flip-flop topology allows the duty cycle on the AS3844/5 to be guaranteed between 49 and 50%. The AS3843/5 requires less than 0.5 mA of start-up current over the full temperature range.

Ordering Information

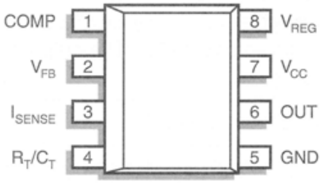
Description	Temperature Range	Order Codes
8-Pin Plastic DIP	0 to 105° C	AS3842/3/4/5N
8-Pin Plastic SOIC	0 to 105° C	AS3842/3/4/5D-8
14-Pin Plastic SOIC	0 to 105° C	AS3842/3/4/5D-14

Pin Configuration — Top view

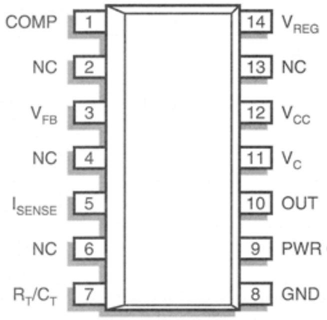
PDIP (N)



8L SOIC (D)



14L SOIC (D)



Functional Block Diagram

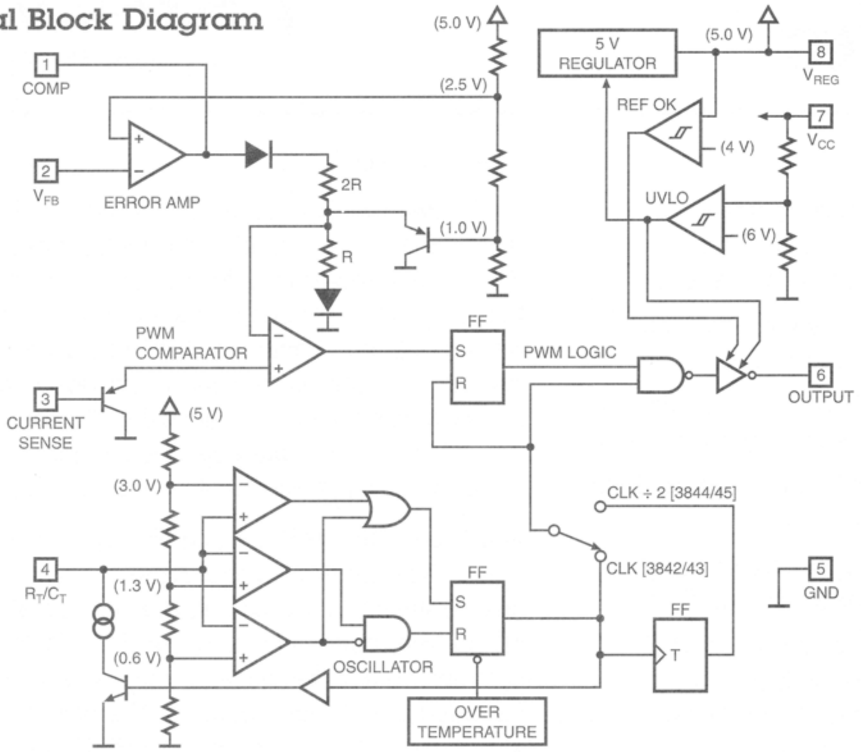


Figure 1. Block Diagram of the AS3842/3/4/5

Pin Function Description

Pin Number	Function	Description
1	COMP	This pin is the error amplifier output. Typically used to provide loop compensation to maintain V_{FB} at 2.5 V.
2	V_{FB}	Inverting input of the error amplifier. The non-inverting input is a trimmed 2.5 V bandgap reference.
3	Current Sense	A voltage proportional to inductor current is connected to the input. The PWM uses this information to terminate the gate drive of the output.
4	R_T/C_T	Oscillator frequency and maximum output duty cycle are set by connecting a resistor (R_T) to V_{REG} and a capacitor (C_T) to ground. Pulling this pin to ground or to V_{REG} will accomplish a synchronization function.
5	GND	Circuit common ground, power ground, and IC substrate.
6	Output	This output is designed to directly drive a power MOSFET switch. This output can sink or source peak currents up to 1A. The output for the AS3844/5 switches at one-half the oscillator frequency.
7	V_{CC}	Positive supply voltage for the IC.
8	V_{REG}	This 5 V regulated output provides charging current for the capacitor C_T through the resistor R_T.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage (I_{CC} < 30 mA)	V_{CC}	Self-Limiting	V
Supply Voltage (Low Impedance Source)	V_{CC}	30	V
Output Current	I_{OUT}	±1	A
Output Energy (Capacitive Load)		5	µJ
Analog Inputs (Pin 2, Pin 3)		−0.3 to 30	V
Error Amp Sink Current		10	mA
Maximum Power Dissipation	P_D		
8L SOIC		750	mW
8L PDIP		1000	mW
14L SOIC		950	mW
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}		
AS3842,4		15	V
AS3843,5		10	V
Oscillator	f_{OSC}	50 to 500	kHz

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
8L PDIP	95° C/W	50° C/W	10.5 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C
14L SOIC	130° C/W	35° C/W	7.7 mW/°C

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{CC} = 15$ V, $R_T = 10$ kΩ, and $C_T = 3.3$ nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5 V Regulator						
Output Voltage	V_{REG}	$T_J = 25°$ C, $I_{REG} = 1$ mA	4.95	5.00	5.05	V
Line Regulation	PSRR	$12 \leq V_{CC} \leq 25$ V		2	10	mV
Load Regulation		$1 \leq I_{REG} \leq 20$ mA		2	10	mV
Temperature Stability[1]	TC_{REG}			0.2	0.4	mV/°C
Total Output Variation[1]		Line, load, temperature	4.85		5.15	V
Long-term Stability[1]		Over 1,000 hrs at 25° C		5	25	mV
Output Noise Voltage	V_{NOISE}	$10 \text{ Hz} \leq f \leq 100$ kHz, $T_J = 25°$ C		50		µV
Short Circuit Current	I_{SC}		30	100	180	mA
2.5 V Internal Reference						
Nominal Voltage	V_{FB}	$T = 25°$ C; $I_{REG} = 1$ mA	2.487	2.500	2.512	V
Line Regulation	PSRR	$12 \text{ V} \leq V_{CC} \leq 25$ V		2	5	mV
Load Regulation		$1 \leq I_{REG} \leq 20$ mA		2	5	mV
Temperature Stability[1]	TC_{VFB}			0.1	0.2	mV/°C
Total Output Variation[1]		Line, load, temperature	2.450	2.500	2.550	V
Long-term Stability[1]		Over 1,000 hrs at 125° C		2	12	mV
Oscillator						
Initial Accuracy	f_{OSC}	$T_J = 25°$ C	47	52	57	kHz
Voltage Stability		$12 \text{ V} \leq V_{CC} \leq 25$ V		0.2	1	%
Temperature Stability[1]	TC_f	$T_{MIN} \leq T_J \leq T_{MAX}$		5		%
Amplitude	f_{OSC}	$V_{RT/CT}$ peak-to-peak		1.6		V
Upper Trip Point	V_H			2.9		V
Lower Trip Point	V_L			1.3		V
Sync Threshold	V_{SYNC}		400	600	800	mV
Discharge Current	I_D		7.5	8.7	9.5	mA
Duty Cycle Limit		$R_T = 680$ Ω, $C_T = 5.3$ nF, $T_J = 25°$ C	46	50	52	%

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error Amplifier						
Input Voltage	V_{FB}	$T_J = 25°$ C	2.470	2.50	2.535	V
Input Bias Current	I_{BIAS}			−0.1	−1	μA
Voltage Gain	A_{VOL}	$2 \leq V_{COMP} \leq 4$ V	65	90	1	dB
Transconductance	G_m			1		mA/mV
Unity Gain Bandwidth[1]	GBW		0.8	1.2		MHz
Power Supply Rejection Ratio	PSRR	$12 \leq V_{CC} \leq 25$ V	60	70		dB
Output Sink Current	I_{COMPL}	V_{FB} = 2.7 V, V_{COMP} = 1.1V	2	6		mA
Output Source Current	I_{COMPH}	V_{FB} = 2.3 V, V_{COMP} = 5 V	0.5	0.8		mA
Output Swing High	V_{COMPH}	V_{FB} = 2.3 V, R_L = 15 kΩ to Ground	5	5.5		V
Output Swing Low	V_{COMPL}	V_{FB} = 2.7 V, R_L = 15 kΩ to Pin 8		0.7	1.1	V
Current Sense Comparator						
Transfer Gain[2,3]	AV_{CS}	$-0.2 \leq V_{SENSE} \leq 0.8$ V	2.85	3.0	3.15	V/V
I_{SENSE} Level Shift[2]	V_{LS}	V_{SENSE} = 0 V		1.5		V
Maximum Input Signal[2]		V_{COMP} = 5 V	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	$12 \leq V_{CC} \leq 25$ V		70		dB
Input Bias Current	I_{BIAS}			−1	−10	μA
Propagation Delay to Output[1]	t_{PD}			85	150	ns
Output						
Output Low Level	V_{OL}	I_{SINK} = 20 mA		0.1	0.4	V
	V_{OL}	I_{SINK} = 200 mA		1.5	2.2	V
Output High Level	V_{OH}	I_{SOURCE} = 20mA	13	13.5		V
	V_{OH}	I_{SOURCE} = 200mA	12	13.5		V
Rise Time[1]	t_R	C_L = 1 nF		50	150	ns
Fall Time[1]	t_F	C_L = 1 nF		50	150	ns
Housekeeping						
Start-up Threshold	V_{CC}(on)	3842/4	15	16	17	V
		3843/5	7.8	8.4	9.0	V
Minimum Operating Voltage After Turn On	V_{CC}(min)	3842/4	9	10	11	V
		3843/5	7.0	7.6	8.2	V
Output Low Level in UV State	V_{OUV}	I_{SINK} = 20 mA, V_{CC} = 6 V		1.5	2.0	V
Over-Temperature Shutdown[4]	T_{OT}			125		°C

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{CC} = 15$ V, $R_T = 10$ kΩ, and $C_T = 3.3$ nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Duty Cycle	D_{max}	3842/3	94	97	100	%
Minimum Duty Cycle	D_{min}	3842/3			0	%
Maximum Duty Cycle	D_{max}	3844/5	49	49.5	50	%
Minimum Duty Cycle	D_{min}	3844/5			0	%
Start-up Current	I_{CC}	3842/4, $V_{FB} = V_{SENSE} = 0$ V, $V_{CC} = 14$ V		0.5	1.0	mA
		3843/5, $V_{FB} = V_{SENSE} = 0$ V, $V_{CC} = 7$ V		0.3	0.5	mA
Operating Supply Current	I_{CC}			9	17	mA
V_{CC} Zener Voltage	V_Z	$I_{CC} = 25$ mA		30		V

Notes:

1. This parameter is not 100% tested in production.
2. Parameter measured at trip point of PWM latch.
3. Transfer gain is the relationship between current sense input and corresponding error amplifier output at the PWM latch trip point and is mathematically expressed as follows:

$$A = \frac{\Delta I_{COMP}}{\Delta V_{SENSE}}; -0.2 \leq \mathrm{V}_{\mathrm{SENSE}} \leq 0.8\ V$$

4. At the over-temperature threshold, T_{OT}, the oscillator is disabled. The 5 V reference and the PWM stages, including the PWM latch, remain powered.

Typical Performance Curves

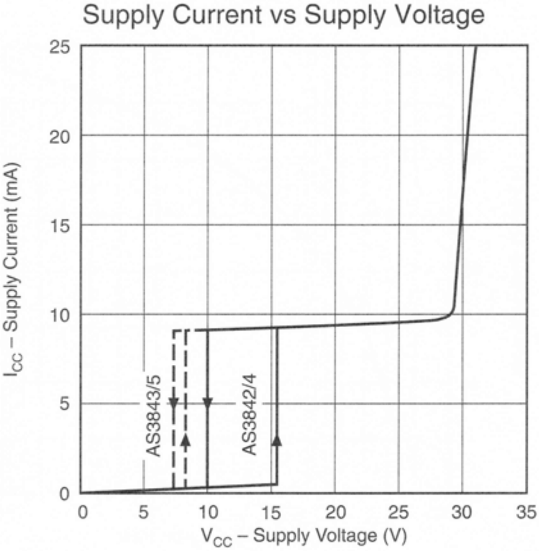

Supply Current vs Supply Voltage

Figure 2

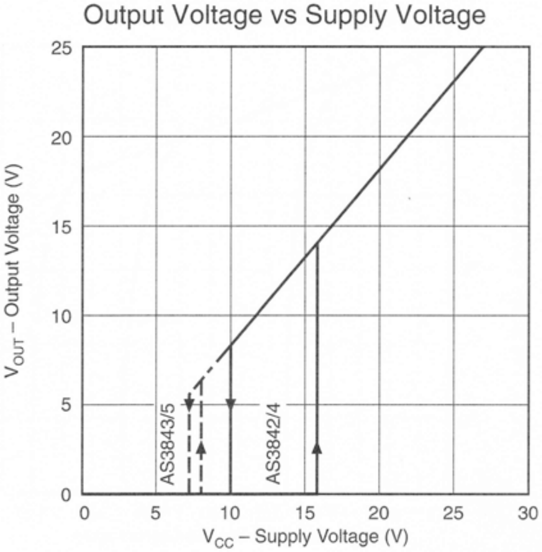

Output Voltage vs Supply Voltage

Figure 3

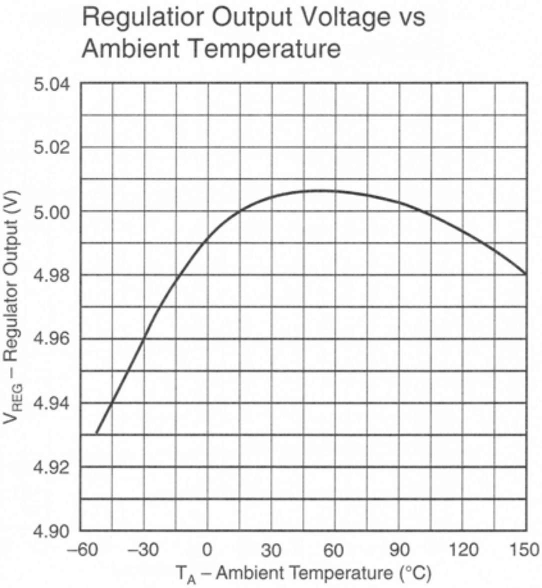

Regulatior Output Voltage vs Ambient Temperature

Figure 4

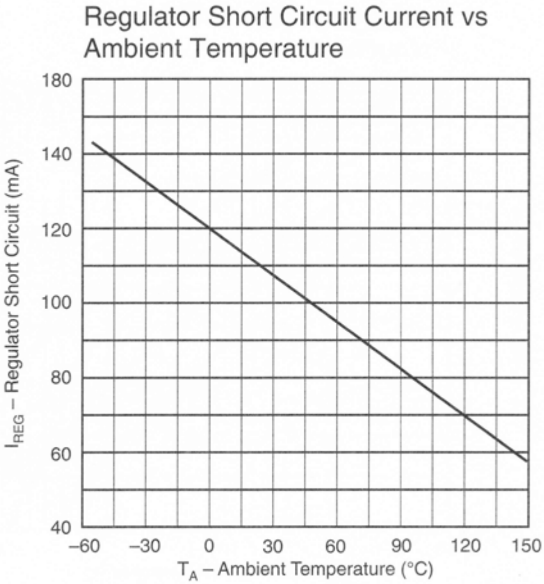

Regulator Short Circuit Current vs Ambient Temperature

Figure 5

Typical Performance Curves

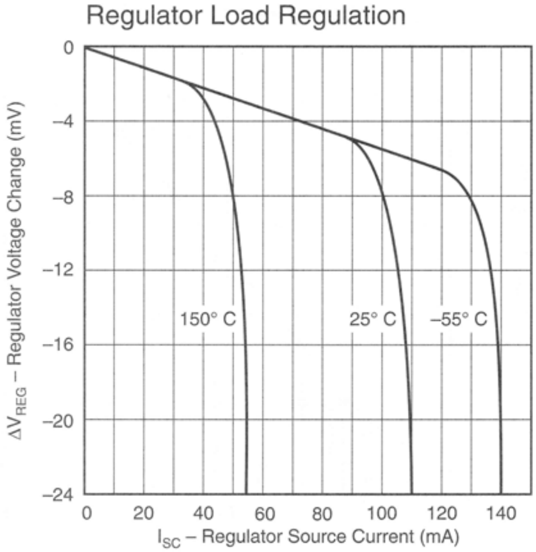

Regulator Load Regulation

Figure 6

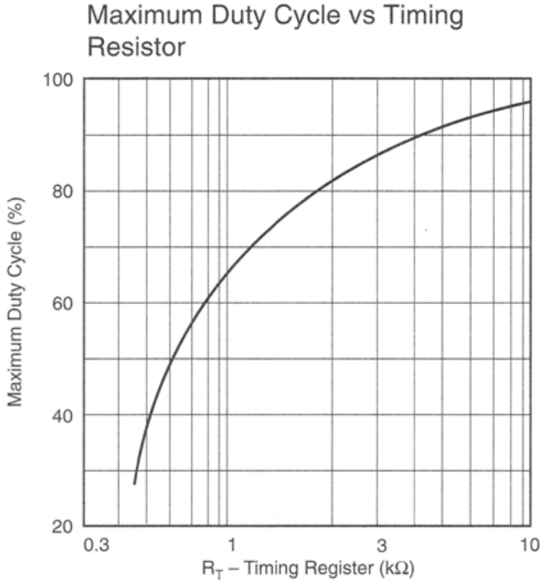

Maximum Duty Cycle vs Timing Resistor

Figure 7

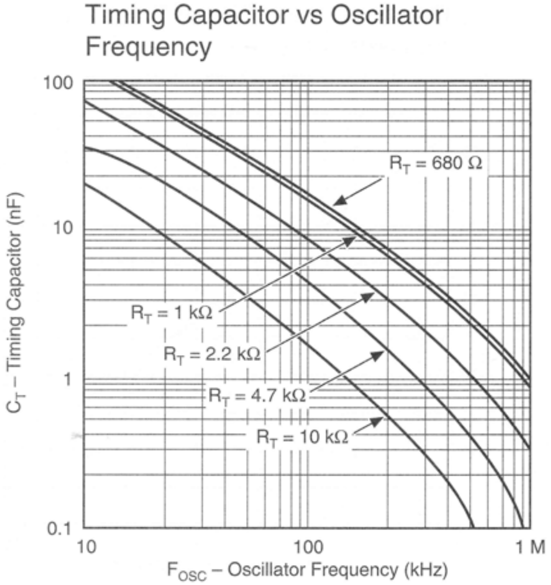

Timing Capacitor vs Oscillator Frequency

Figure 8

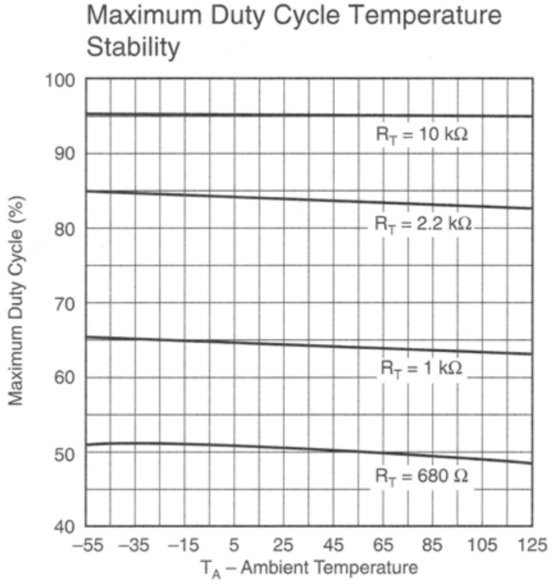

Maximum Duty Cycle Temperature Stability

Figure 9

Typical Performance Curves

Current Sense Input Threshold vs Error Amp Output Voltage

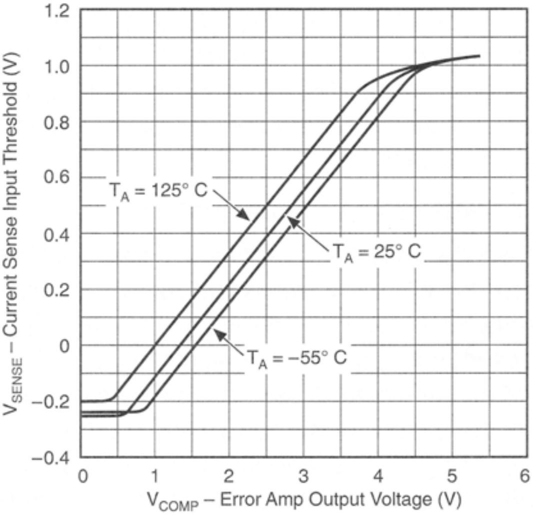


Figure 10

Error Amp Input Voltage vs Ambient Temperature

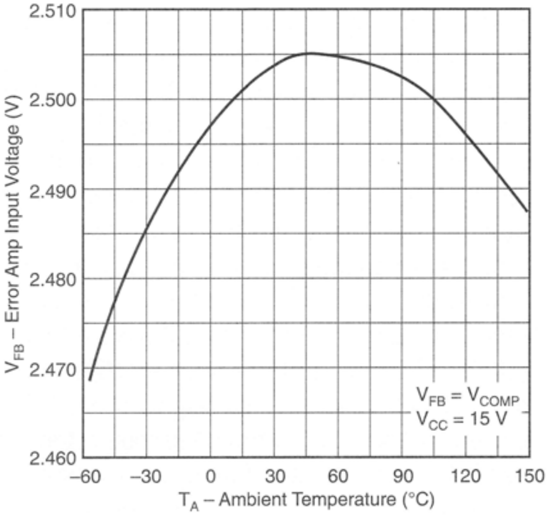


Figure 11

Output Sink Capability In Under-Voltage Mode

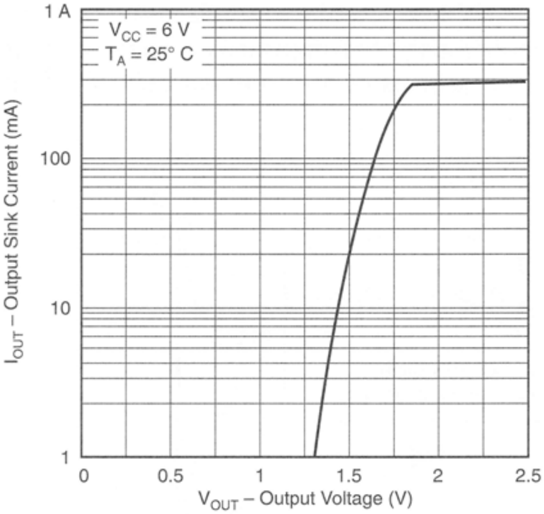


Figure 12

Output Saturation Voltage

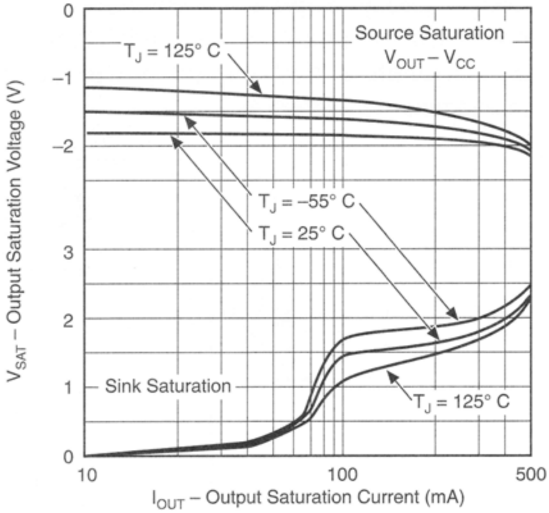


Figure 13

Application Information

The AS3842/3/4/5 family of current-mode control ICs are low cost, high performance controllers which are pin compatible with the industry standard UC3842 series of devices. Suitable for many switch mode power supply applications, these ICs have been optimized for use in high frequency off-line and DC-DC converters. The AS3842 has been enhanced to provide significantly improved performance, resulting in exceptionally better tolerances in power supply manufacturing. In addition, all electrical characteristics are guaranteed over the full 0 to 105 °C temperature range. Among the many enhancements are: a precision trimmed 2.5 volt reference (±0.5% of nominal at the error amplifier input), a significantly reduced propagation delay from current sense input to the IC output, a trimmed oscillator for precise duty-cycle clamping, a modified flip-flop scheme that gives a true 50% duty ratio clamp on 3844/45 types, and an improved 5 V regulator for better AC noise immunity. Furthermore, the AS3842 provides guaranteed performance with current sense input below ground. The advanced oscillator design greatly simplifies synchronization. The device is more completely specified to guarantee all parameters that impact power supply manufacturing tolerances.

Section 1— Theory of Operation

The functional block diagram of the AS3842 is shown in Figure 01. The IC is comprised of the six basic functions necessary to implement current mode control; the under-voltage lockout; the reference; the oscillator; the error amplifier; the current sense comparator/PWM latch; and the output. The following paragraphs will describe the theory of operation of each of the functional blocks.

1.1 Under-voltage lockout (UVLO)

The under-voltage lockout function of the AS3842 holds the IC in a low quiescent current (≤ 1 mA) "standby" mode until the supply voltage (V_{CC}) exceeds the upper UVLO threshold voltage. This guarantees that all of the IC's internal circuitry are properly biased and fully functional before the output stage is enabled. Once the IC turns on, the UVLO threshold shifts to a lower level (hysteresis) to prevent V_{CC} oscillations.

The low quiescent current standby mode of the AS3842 allows "bootstrapping"—a technique used in off-line converters to start the IC from the rectified AC line voltage initially, after which power to the IC is provided by an auxiliary winding off the power supply's main transformer. Figure 14 shows a typical bootstrap circuit where capacitor (C) is

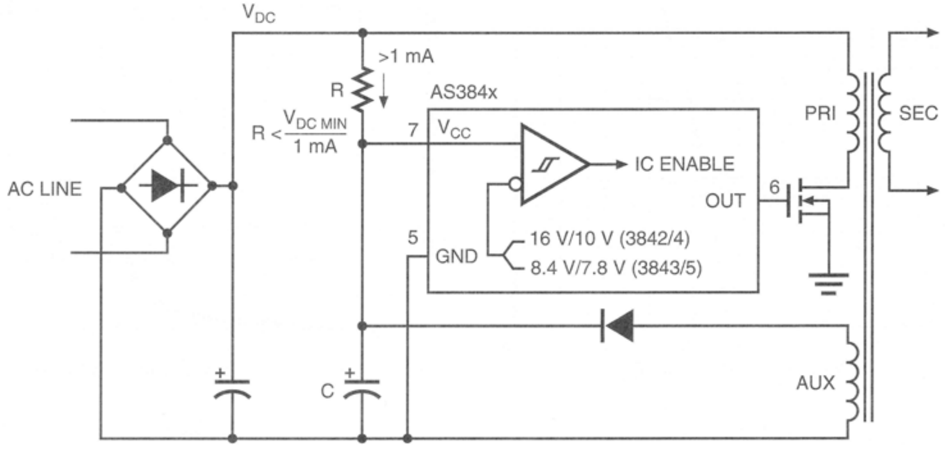


Figure 14. Boostrap Circuit

charged via resistor (R) from the rectified AC line. When the voltage on the capacitor (V_{CC}) reaches the upper UVLO threshold, the IC (and hence, the power supply) turns on and the voltage on C begins to quickly discharge due to the increased operating current. During this time, the auxiliary winding begins to supply the current necessary to run the IC. The capacitor must be sufficiently large to maintain a voltage greater than the lower UVLO threshold during start up. The value of R must be selected to provide greater than 1 mA of current at the minimum DC bus voltage (R < VDCmin/1 mA).

The UVLO feature of the AS3842 has significant advantages over standard 3842 devices. First, the UVLO thresholds are based on a temperature compensated band gap reference rather than conventional zeners. Second, the UVLO disables the output at power down, offering additional protection in cases where V_{REG} is heavily decoupled. The UVLO on some 3842 devices shuts down the 5 volt regulator only, which results in eventual power down of the output only after the 5 volt rail collapses. This can lead to unwanted stresses on the switching devices during power down. The AS3842 has two separate comparators which monitor both V_{CC} and V_{REF} and hold the output low if either are not within specification.

The AS3842 family offers two different UVLO options. The AS3842/4 has UVLO thresholds of 16 volts (on) and 10 volts (off). The AS3843/5 has UVLO levels of 8.4 volts (on) and 7.6 volts (off).

1.2 Reference (V_{REG} and V_{FB})

The AS3842 effectively has two precise band gap based temperature compensated voltage references. Most obvious is the V_{REG} pin (pin 8) which is the output of a series pass regulator. This 5.0 V output is normally used to provide charging current to the oscillator's timing capacitor (Section 1.3). In addition, there is a trimmed internal 2.5 V reference which is connected to the non-inverting (+) input of the error amplifier. The tolerance of the internal reference is ±0.5% over the full specified temperature range, and ±1% for V_{REG}.

The reference section of the AS3842 is greatly improved over the standard 3842 in a number of ways. For example, in a closed loop system, the voltage at the error amplifier's inverting input (V_{FB}, pin 1) is forced by the loop to match the voltage at the non-inverting input. Thus, V_{FB} is the voltage which sets the accuracy of the entire system. The 2.5 V reference of the AS3842 is tightly trimmed for precision at V_{FB}, including errors caused by the op amp, and is specified over temperature. This method of trim provides a precise reference voltage for the error amplifier while maintaining the original 5 V regulator specifications. In addition, force/sense (Kelvin) bonding to the package pin is utilized to further improve the 5 V load regulation. Standard 3842's, on the other hand, specify tight regulation for the 5 V output only and rate it over line, load and temperature. The voltage at V_{FB}, which is of critical importance, is loosely specified and only at 25° C.

The reference section, in addition to providing a precise DC reference voltage, also powers most of the IC's internal circuitry. Switching noise, therefore, can be internally coupled onto the reference. With this in mind, all of the logic within the AS3842 was designed with ECL type circuitry which generates less switching noise because it runs at essentially constant current regardless of logic state. This, together with improved AC noise rejection, results in substantially less switching noise on the 5 V output.

The reference output is short circuit protected and can safely deliver more than 20 mA to power external circuitry.

1.3 Oscillator

The newly designed oscillator of the AS3842 is enhanced to give significantly improved performance. These enhancements are discussed in the following paragraphs. The basic operation of the oscillator is as follows:

A simple RC network is used to program the frequency and the maximum duty ratio of the AS3842 output. See Figure 15. Timing capacitor (C_T) is charged through timing resistor (R_T) from the fixed 5.0 V at V_{REG}. During the charging time, the OUT (pin 6) is high. Assuming that the output is not terminated by the PWM latch, when the voltage across C_T reaches the upper oscillator trip point (≈3.0 V), an internal current sink from pin 4 to ground is turned on and discharges C_T towards the lower trip point. During this discharge time, an internal clock pulse blanks the output to its low state. When the voltage across C_T reaches the lower trip point (≈1.3 V), the current sink is turned off, the output goes high, and the cycle repeats. Since the output is blanked during the discharge of C_T, it is the discharge time which controls the output deadtime and hence, the maximum duty ratio.

The nature of the AS3842 oscillator circuit is such that, for a given frequency, many combinations of R_T and C_T are possible. However, only one value of R_T will yield the desired maximum duty ratio at a given frequency. Since a precise maximum duty ratio clamp is critical for many power supply designs, the oscillator discharge current is trimmed in a unique manner which provides significantly improved tolerances as explained later in this section. In addition, the AS3844/5 options have an internal flip-flop which effectively blanks every other output pulse (the oscillator runs at twice the output frequency), providing an absolute maximum 50% duty ratio regardless of discharge time.

1.3.1 Selecting timing components R_T and C_T

The values of R_T and C_T can be determined mathematically by the following expressions:

$$C_T = \frac{D}{R_T f_{OSC} \ln\left(\frac{K_L}{K_H}\right)} = \frac{1.63D}{R_T f_{OSC}} \qquad (1)$$

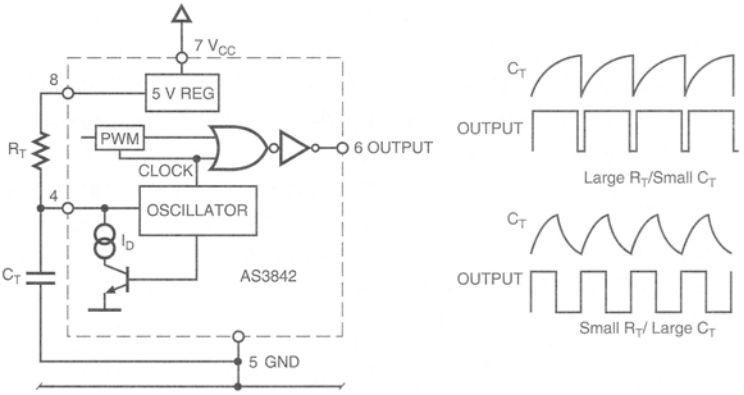


Figure 15. Osillator Set-up and Waveforms

$$R_T = \frac{V_{REG}}{I_D} \cdot \frac{(K_L)^{\frac{1}{D}} - (K_H)^{\frac{1}{D}}}{(K_L)^{\frac{1-D}{D}} - (K_H)^{\frac{1-D}{D}}} \qquad (2)$$

$$= 582 \cdot \frac{(0.736)^{\frac{1}{D}} - (0.432)^{\frac{1}{D}}}{(0.736)^{\frac{1-D}{D}} - (0.432)^{\frac{1-D}{D}}}$$

$$\mathrm{K_L} = \frac{\mathrm{V_{REG}} - V_L}{V_{REG}} \approx 0.736 \qquad (3)$$

$$\mathrm{K_H} = \frac{\mathrm{V_{REG}} - V_H}{V_H} \approx 0.432 \qquad (4)$$

where f_{osc} is the oscillator frequency, D is the maximum duty ratio, V_H is the oscillator's upper trip point, V_L is the lower trip point, V_R is the Reference voltage, I_D is the discharge current.

Table 1 lists some common values of R_T and the corresponding maximum duty ratio. To select the timing components; first, use Table 1 or equation (2) to determine the value of R_T that will yield the desired maximum duty ratio. Then, use equation (1) to calculate the value of C_T. For example, for a switching frequency of 250 kHz and a maximum duty ratio of 50%, the value of R_T, from Table 1, is 683 Ω. Applying this value to equation (1) and solving for C_T gives a value of 4700 pF. In practice, some fine tuning of the initial values may be necessary during design. However, due to the advanced design of the AS3842 oscillator, once the final values are determined, they will yield repeatable results, thus eliminating the need for additional trimming of the timing components during manufacturing.

Table 1. R_T vs Maximum Duty Ratio

R_T (Ω)	Dmax
470	22%
560	37%
683	50%
750	54%
820	58%
910	63%
1,000	66%
1,200	72%
1,500	77%
1,800	81%
2,200	85%
2,700	88%
3,300	90%
3,900	91%
4,700	93%
5,600	94%
6,800	95%
8,200	96%
10,000	97%
18,000	98%

1.3.2 Oscillator enhancements

The AS3842 oscillator is trimmed to provide guaranteed duty ratio clamping. This means that the discharge current (I_D) is trimmed to a value that compensates for all of the tolerances within the device (such as the tolerances of V_{REG}, propagation delays, the oscillator trip points, etc.) which have an effect on the frequency and maximum duty ratio. For example, if the combined tolerances of a particular device are 0.5% above nominal, then I_D is trimmed to 0.5% above nominal. This method of trimming virtually eliminates the need to trim external oscillator components during power supply manufacturing. Standard 3842 devices specify or trim only for a specific value of discharge current. This makes precise and repeatable duty ratio clamping virtually impossible due to other IC tolerances. The AS3844/5 provides true 50% duty ratio clamping by virtue of excluding from its flip-flop scheme, the normal output blanking associated with the discharge of C_T. Standard AS3844/5 devices include the output blanking associated with the discharge of C_T, resulting in somewhat less than a 50% duty ratio.

1.3.3 Synchronization

The advanced design of the AS3842 oscillator simplifies synchronizing the frequency of two or more devices to each other or to an external clock. The R_T/C_T doubles as a synchronization input which can easily be driven from any open collector logic output. Figure 16 shows some simple circuits for implementing synchronization.

1.4 Error amplifier (COMP)

The AS3842 error amplifier is a wide bandwidth, internally compensated operational amplifier which provides a high DC open loop gain (90 dB). The input to the amplifier is a PNP differential pair. The non-inverting (+) input is internally connected to the 2.5 V reference, and the inverting (–) input is available at pin 2 (V_{FB}). The output of the error amplifier consists of an active pull-down and a 0.8 mA current source pull-up as shown in Figure 17. This type of output stage allows easy implementation of soft start, latched shutdown and reduced current sense clamp functions. It also permits wire “OR-ing” of the error amplifier outputs of several 3842s, or complete bypass of the error amplifier when its output is forced to remain in its “pull-up” condition.

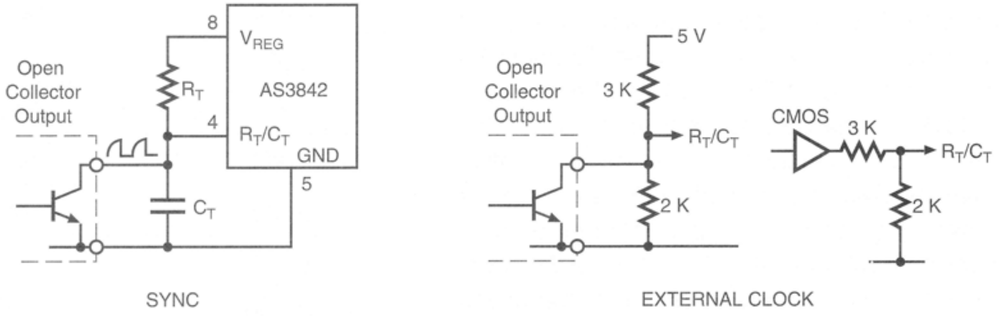


Figure 16. Synchronization

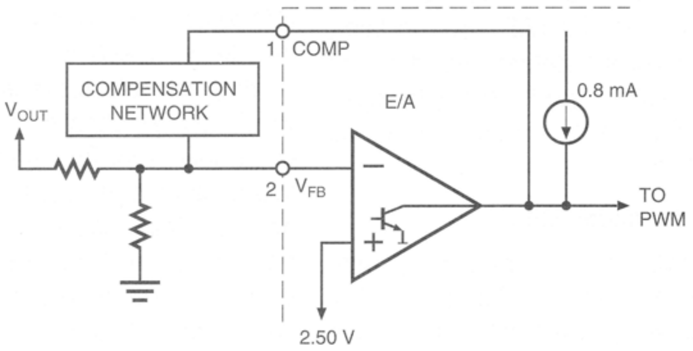


Figure 17. Error Amplifier Compensation

In most typical power supply designs, the converter's output voltage is divided down and monitored at the error amplifier's inverting input, V_{FB}. A simple resistor divider network is used and is scaled such that the voltage at V_{FB} is 2.5 V when the converter's output is at the desired voltage. The voltage at V_{FB} is then compared to the internal 2.5 V reference and any slight difference is amplified by the high gain of the error amplifier. The resulting error amplifier output is level shifted by two diode drops and is then divided by three to provide a 0 to 1 V reference (V_E) to one input of the current sense comparator. The level shifting reduces the input voltage range of the current sense input and prevents the output from going high when the error amplifier output is forced to its low state. An internal clamp limits V_E to 1.0 V. The purpose of the clamp is discussed in Section 1.5.

1.4.1 Loop compensation

Loop compensation of a power supply is necessary to ensure stability and provide good line/load regulation and dynamic response. It is normally provided by a compensation network connected between the error amplifier's output (COMP) and inverting input as shown in Figure 17. The type of network used depends on the converter topology and in particular, the characteristics of the major functional blocks within the supply - i.e. the error amplifier, the modulator/switching circuit, and the output filter. In general, the network is designed such that the converters overall gain/phase response approaches that of a single pole with a –20 dB/decade rolloff, crossing unity gain at the highest possible frequency (up to $f_{SW}/4$) for good dynamic response, with adequate phase margin (> 45°) to ensure stability.

Figure 18 shows the Gain/Phase response of the error amplifier. The unity gain crossing is at 1.2 MHz with approximately 57° C of phase margin. This information is useful in determining the configuration and characteristics required for the compensation network.

One of the simplest types of compensation networks is shown in Figure 19. An RC network provides a single pole which is normally set to compensate for the zero introduced by the the output capacitor's ESR. The frequency of the pole (f_P) is determined by the formula;

$$f_P = \frac{1}{2\pi\, R_f\, C_f} \tag{5}$$

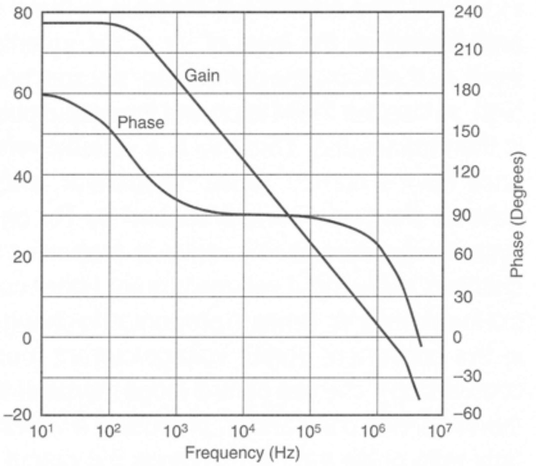


Figure 18. Gain/Phase Response of the AS3842

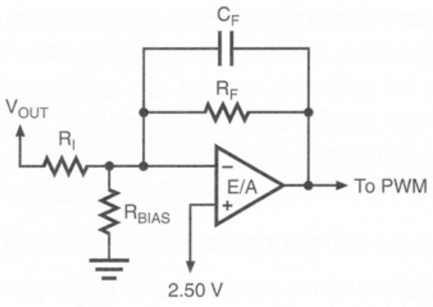


Figure 19. A Typical Compensation Network

Resistors R_1 and R_F set the low frequency gain and should be chosen to provide the highest possible gain, without exceeding the unity gain crossing frequency limit of f_{SW} /4. R_{BIAS}, in conjunction with R_1, sets the converter's output voltage; but has no effect on the loop gain/phase response.

There are a few converter design considerations associated with the error amplifier. First, the values of the divider network (R_1 and R_{BIAS}) should be kept low in order to minimize errors caused by the error amplifier's input bias current ($\approx -3.0\ \mu A$). An output voltage error equal to the product of the input bias current and the equivalent divider resistance, can be quite significant with divider values greater than 5 kΩ. Low divider resistor values also help to improve the noise immunity of the sensitive V_{FB} input.

The second consideration is that the error amplifier will typically source only 0.8 mA; thus, the value of feedback resistance (R_F) should be no lower than 5 kΩ in order to maintain the error amplifier's full output range. In practice, however, the feedback resistance required is usually much greater than 5 kΩ, hence this limitation is normally not a problem.

Some power supply topologies may require a more elaborate compensation network. For example, flyback and boost converters operating with continuous current have transfer functions that include a right half plane (RHP) zero. These types of systems require an additional pole element within the compensation network. A detailed discussion of loop compensation, however, is beyond the scope of this application note.

1.5 I_{SENSE} current comparator/PWM latch

The current sense comparator (sometimes called the PWM comparator) and accompanying latch circuitry make up the pulse width modulator (PWM). It provides pulse-by-pulse current sensing/limiting and generates a variable duty ratio pulse train which controls the output voltage of the power supply. Included is a high speed comparator followed by ECL type logic circuitry which has very low propagation delays and switching noise. This is essential for high frequency power supply designs. The comparator has been designed to provide guaranteed performance with the current sense input below ground. The PWM latch ensures that only one pulse is allowed at the output for each oscillator period.

The inverting input to the current sense comparator is internally connected to the level shifted output of the error amplifier (V_E) as discused in the previous section. The non-inverting input is the I_{SENSE} input (pin 3). It monitors the switched inductor current of the converter.

Figure 20 shows the current sense/PWM circuitry of the AS3842, and associated waveforms. The output is set high by an internal clock pulse and remains high until one of two conditions occur; 1) the oscillator times out (Section 1.3 or 2) the PWM latch is set by the current sense comparator. During the time when the output is high, the converter's switching device is turned on and current flows through resistor R_S. This produces a stepped ramp waveform at pin 3 as shown in Figure 20. The current will continue to ramp up until it reaches the level of V_E at the inverting input. At that point, the comparator's output goes high, setting the PWM latch and the output pulse is then terminated. Thus, V_E is a variable reference for the current sense comparator, and it controls the peak current sensed by R_S on a cycle-by-cycle basis. V_S varies in proportion to changes in the input voltage/current (inner control loop) while V_E varies in proportion to changes in the converters output voltage/current (outer control loop). The two control loops merge at the current sense comparator, producing a variable duty ratio pulse train that controls the output of the converter.

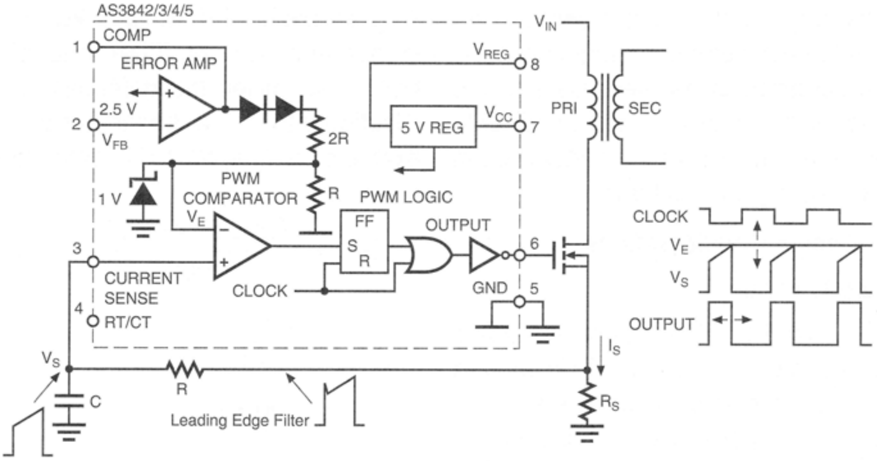


Figure 20. Current Sense/PWN Latch Circuit and Waveforms

The current sense comparator's inverting input is internally clamped to a level of 1.0 V to provide a current limit (or power limit for multiple output supplies) function. The value of R_S is selected to produce 1.0 V at the maximum allowed current. For example, if 1.5 A is the maximum allowed peak inductor current, then R_S is selected to equal 1 V/1.5 A = 0.66 Ω. In high power applications, power dissipation in the current sense resistor may become intolerable. In such a case, a current transformer can be used to step down the current seen by the sense resistor. See Figure 21.

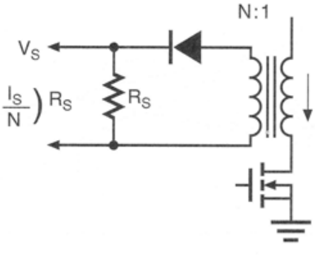


Figure 21. Optional Current Transformer

1.6 Output (OUT)

The output stage of the AS3842 is a high current totem-pole configuration that is well suited for directly driving power MOSFETs. It is capable of sourcing and sinking up to 1 A of peak current. Cross conduction losses in the output stage have been minimized resulting in lower power dissipation in the device. This is particularly important for high frequency operation. During under-voltage shutdown conditions, the output is active low. This eliminates the need for an external pulldown resistor.

1.7 Over-temperature shutdown

The AS3842 has a built-in over-temperature shutdown which will limit the die temperature to 130° C typically. When the over-temperature condition is reached, the oscillator is disabled. All other circuit blocks remain operational. Therefore, when the oscillator stops running, output pulses terminate without losing control of the supply or losing any peripheral functions that may be running off the 5 V regulator. The output may go high during the final cycle, but the PWM latch is still fully operative, and the normal termination of this cycle by the current sense comparator will latch the output low until the over-temperature condition is rectified. Cycling the power will reset the over-temperature disable mechanism, or the chip will re-start after cooling through a nominal hysteresis band.

Section 2 – Design Considerations

2.1 Leading edge filter

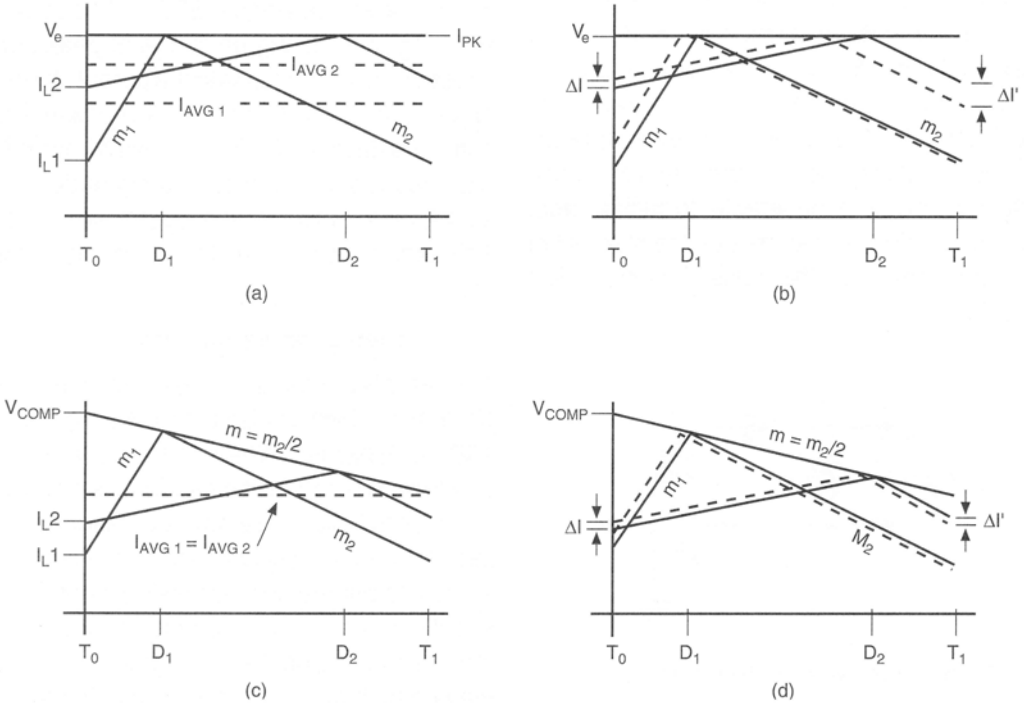
The current sensed by R_S contains a leading edge spike as shown in Figure 20. This spike is caused by parasitic elements within the circuit including the interwinding capacitance of the power transformer and the recovery characteristics of the rectifier diode(s). The spike, if not properly filtered, can cause stability problems by prematurely terminating the output pulse.

A simple RC filter is used to suppress the spike. The time constant should be chosen such that it approximately equals the duration of the spike. A good choice for R_1 is 1 kΩ, as this value is optimum for the filter and at the same time, it simplifies the determination of R_{SLOPE} (Section 2.2). If the duration of the spike is, for example, 100 ns, then C is determined by:

$$\begin{aligned} C &= \frac{\text{Time Constant}}{1\ \text{k}\Omega} \\ &= \frac{100\ \text{ns}}{1\ \text{k}\Omega} \\ &= 100\ \text{pF} \end{aligned} \tag{6}$$

2.2 Slope compensation

Current-mode controlled converters can experience instabilities or subharmonic oscillations when operated at duty ratios greater than 50%. Two different phenomena can occur as shown



(a) (b) (c) (d)

Figure 22. Slope Compensation

graphically in Figure 22.

First, current-mode controllers detect and control the peak inductor current, where as the converter's output corresponds to the average inductor current. Figure 22(a) clearly shows that the average inductor current (I_1 & I_2) changes as the duty ratio (D_1 & D_2) changes. Note that for a fixed control voltage, the peak current is the same for any duty ratio. The difference between the peak and average currents represents an error which causes the converter to deviate from true current-mode control.

Second, Figure 22(b) depicts how a small perturbation of the inductor current (ΔI) can result in an unstable condition. For duty ratios less than 50 %, the disturbance will quickly converge to a steady state condition. For duty ratios greater than 50 %, ΔI progressively increases on each cycle, causing an unstable condition.

Both of these problems are corrected simultaneously by injecting a compensating ramp into either the control voltage (V_E) as shown in Figure 22(c) & (d), or to the current sense waveform at pin 3. Since V_E is not directly accessible, and, a positive ramp waveform is readily available from the oscillator at pin 4, it is more practical to add the slope compensation to the current waveform. This can be implemented quite simply with the addition of a single resistor, R_{SLOPE}, between pin 4 and pin 3 as shown in Figure 23(a). R_{SLOPE}, in conjunction with the leading edge filter resistor, R_1 (Section 2.1), forms a divider network which determines the amount of slope added to the waveform. The amount of slope added to the current waveform is inversely proportional to the value of R_{SLOPE}. It has been determined that the amount of slope (m) required is equal to or greater than 1/2 the downslope (m_2) of the inductor current. Mathematically stated:

$$m \geq \frac{m_2}{2} \tag{7}$$

In some cases the required value of R_{SLOPE} may be low enough to affect the oscillator circuit and thus cause the frequency to shift. An emitter follower circuit can be used as a buffer for R_{SLOPE} as depicted in Figure 23(b).

Slope compensation can also be used to improve noise immunity in current mode converters operating at less than 50% duty ratio. Power supplies

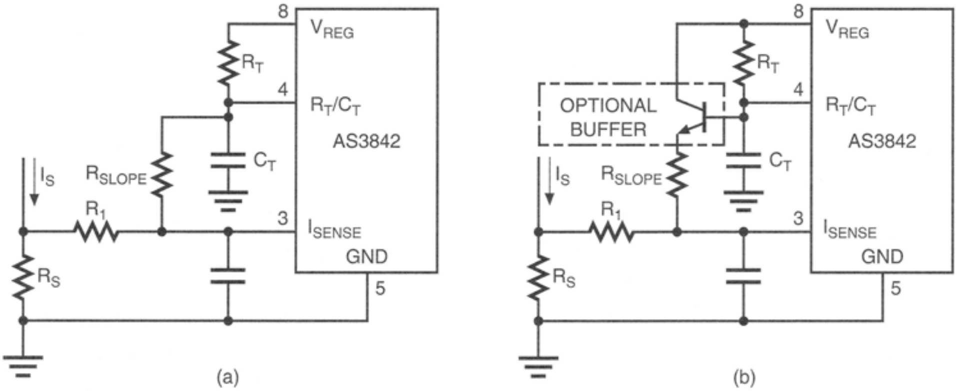


Figure 23. Slope Compensation

operating under very light load can experience instabilities caused by the low amplitude of the current sense ramp waveform. In such a case, any noise on the waveform can be sufficient to trip the comparator resulting in random and premature pulse termination. The addition of a small amount of artificial ramp (slope compensation) can eliminate such problems without drastically affecting the overall performance of the system.

2.3 Circuit layout and other considerations

The eletronic noise generated by any switch-mode power supply can cause severe stability problems if the circuit is not layed-out (wired) properly. A few simple layout practices will help to minimize noise problems.

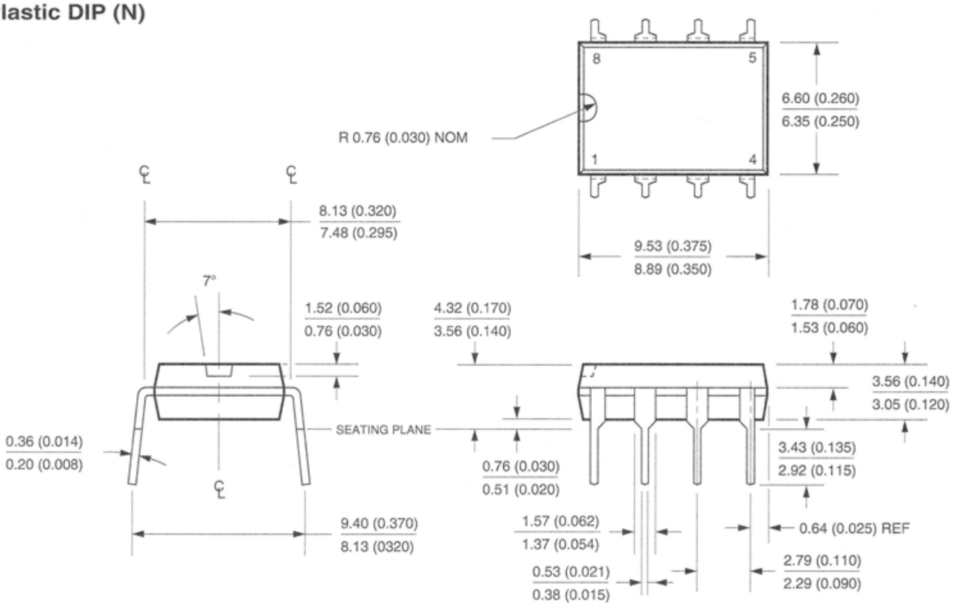
When building prototype breadboards, never use plug-in protoboards or wire wrap construction. For best results, do all breadboarding on double sided PCB using ground plane techniques. Keep all traces and lead lengths to a minimum. Avoid large loops and keep the area enclosed within any loops to a minimum. Use common point grounding techniques and separate the power ground traces from the signal ground traces. Locate the control IC and circuitry away from switching devices and magnetics. Also, the timing capacitor's ground connection must be right at pin 5 as shown in Figure 15. These grounding and wiring techniques are very important because the resistance and inductance of the traces are significant enough to generate noise glitches which can disrupt the normal operation of the IC.

Also, to provide a low impedance path for high frequency noise, V_{CC} and V_{REF} should be decoupled to IC ground with 0.1 μF capacitors. Additional decoupling in other sensitive areas may also be necessary. It is very important to locate the decoupling capacitors as close as possible to the circuit being decoupled.

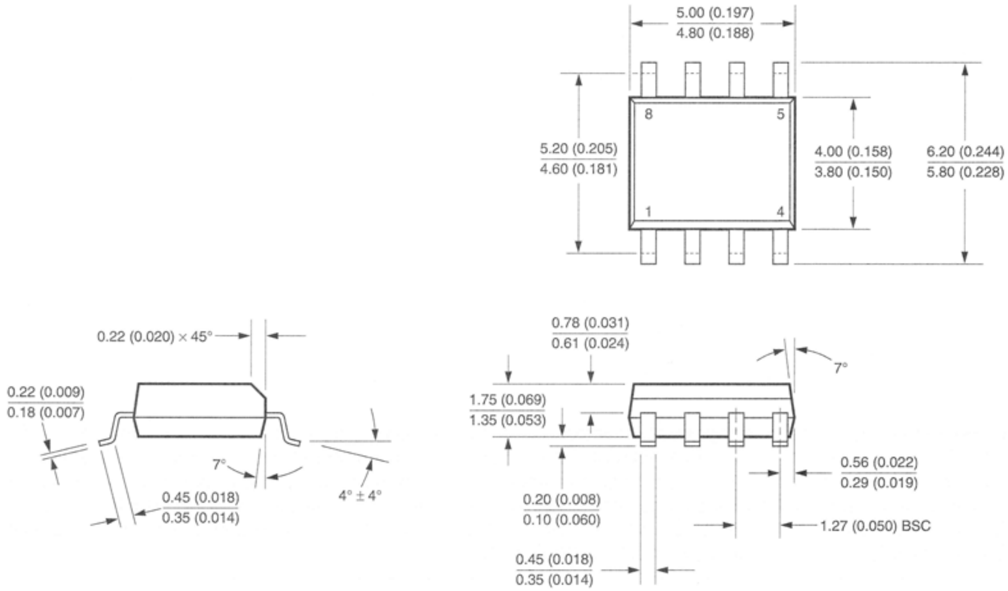
Package Dimensions

All Dimensions in mm (Inches)

8-Pin Plastic DIP (N)



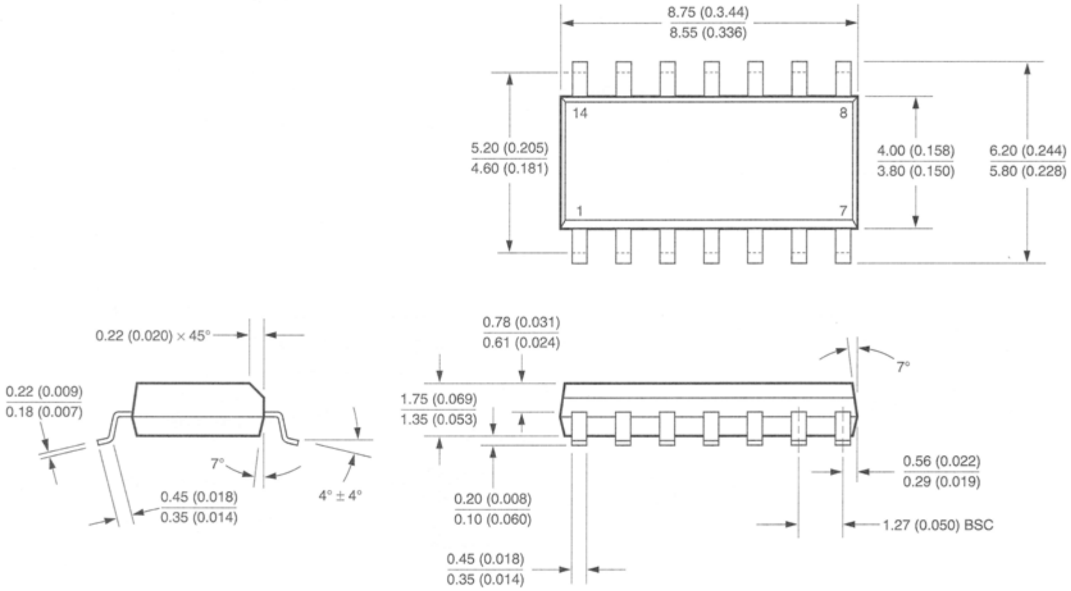
8-Pin Plastic SOIC (D)



Package Dimensions

All Dimensions in mm (Inches)

14-Pin Plastic SOIC (D)



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ASTEC

UC2842/3/4/5

Current Mode Controller

Preliminary Specification

Features

- 2.5 V bandgap reference trimmed to 1% and temperature compensated
- UC2842/3 oscillators trimmed for precision duty cycle clamp
- Improved specs on UVLO and hysteresis provide more predictable start-up and shut-down
- Improved 5 V regulator provides better AC noise immunity
- Guaranteed performance with I_{SENSE} pulled below ground
- Over-temperature shutdown
- Current mode operation to 500 kHz
- Low start-up and operating current
- Low cost

Description

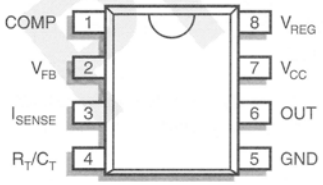
The UC2842/3/4/5 family of control IC's are fixed frequency current mode pulse width modulation controllers. They provide all the features necessary to implement off-line or DC to DC convertor applications with a minimal number of external components.These circuits include a precision bandgap reference trimmed for 1% accuracy at the error amp input, a trimmed oscillator discharge current for precise maximum duty cycle control, a high gain error amplifier, a PWM comparator providing cycle-by-cycle current limit control and a high current totem pole output for driving power MOSFETs.

The UC2842 and UC2844 have under-voltage lockout thresholds of 16V (on) and 10V (off), making them ideal for off-line applications. The UC2843 and UC2845 have UVLO thresholds of 8.4V (on) and 7.6V (off), and require less than 0.5 mA of startup current. The UC2842 and UC2843 operates at duty cycles near 100%. The UC2844/45 have a maximum duty cycle range from 0% to 50%, due to an internal flip-flop that blanks the output at every other clock cycle.

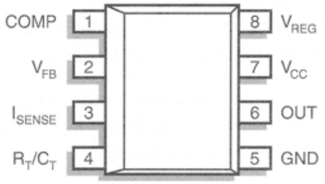
PRELIMINARY

Pin Configuration — Top view

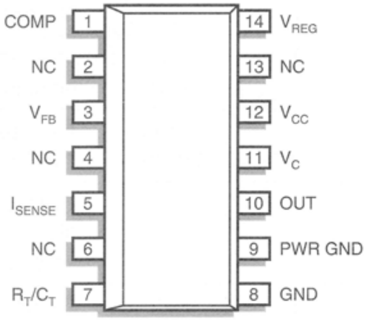
PDIP (N)



8L SOIC (D)



14L SOIC (D)



Ordering Information

Description	Temperature Range	Order Codes
8-Pin Plastic DIP	-40 to 85° C	UC2842/3/4/5N
8-Pin Plastic SOIC	-40 to 85° C	UC2842/3/4/5D-8
14-Pin Plastic SOIC	-40 to 85° C	UC2842/3/4/5D-14

Functional Block Diagram

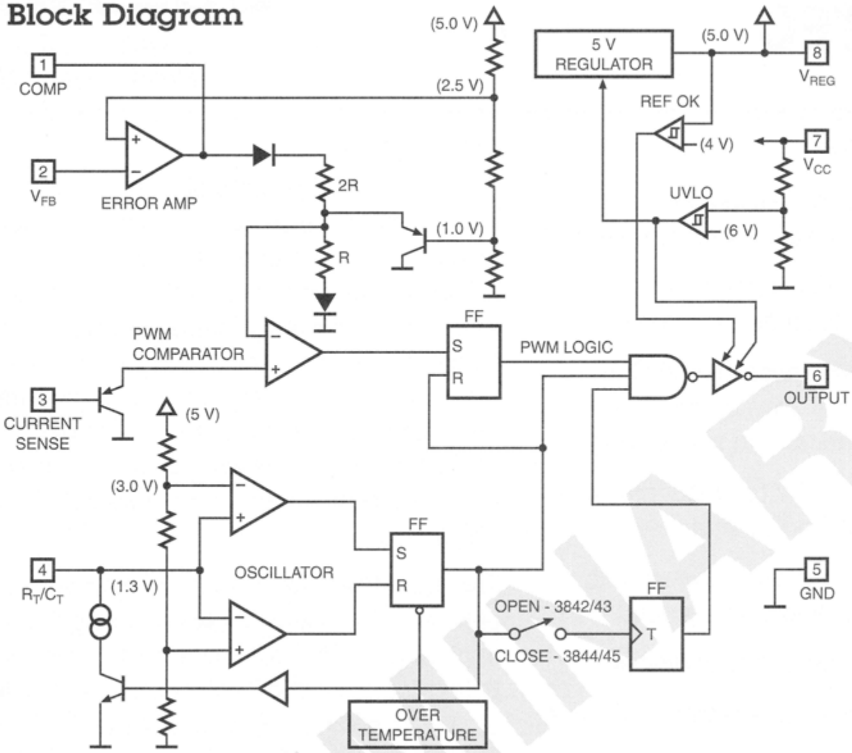


Figure 1. Block Diagram of the UC2842/3/4/5

Pin Function Description

Pin Number	Function	Description
1	COMP	This pin is the error amplifier output. Typically used to provide loop compensation to maintain V_{FB} at 2.5 V.
2	V_{FB}	Inverting input of the error amplifier. The non-inverting input is a trimmed 2.5 V bandgap reference.
3	Current Sense	A voltage proportional to inductor current is connected to the input. The PWM uses this information to terminate the gate drive of the output.
4	R_T/C_T	Oscillator frequency and maximum output duty cycle are set by connecting a resistor (R_T) to V_{REG} and a capacitor (C_T) to ground. Pulling this pin to ground or to V_{REG} will accomplish a synchronization function.
5	GND	Circuit common ground, power ground, and IC substrate.
6	Output	This output is designed to directly drive a power MOSFET switch. This output can sink or source peak currents up to 1A. The output for the UC2844/5 switches at one-half the oscillator frequency.
7	V_{CC}	Positive supply voltage for the IC.
8	V_{REG}	This 5 V regulated output provides charging current for the capacitor C_T through the resistor R_T.

PRELIMINARY

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage (I_{CC} < 30 mA)	V_{CC}	Self-Limiting	V
Supply Voltage (Low Impedance Source)	V_{CC}	30	V
Output Current	I_{OUT}	±1	A
Output Energy (Capacitive Load)		5	µJ
Analog Inputs (Pin 2, Pin 3)		−0.3 to 30	V
Error Amp Sink Current		10	mA
Maximum Power Dissipation	P_D		
8L SOIC		750	mW
8L PDIP		1000	mW
14L SOIC		950	mW
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PRELIMINARY

Recommended Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}		
UC2842,4		15	V
UC2843,5		10	V
Oscillator	f_{OSC}	50 to 500	kHz

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
8L PDIP	95° C/W	50° C/W	10.5 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C
14L SOIC	130° C/W	35° C/W	7.7 mW/°C

Electrical Characteristics

Electrical characteristics are guaranteed over full junction temperature range (-40 to 85° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5 V Regulator						
Output Voltage	V_{REG}	T_J = 25° C, I_{REG} = 1 mA	4.95	5.00	5.05	V
Line Regulation	PSRR	$12 \le V_{CC} \le 25$ V		2	10	mV
Load Regulation		$1 \le I_{REG} \le 20$ mA		2	10	mV
Temperature Stability[1]	TC_{REG}			0.2	0.4	mV/°C
Total Output Variation[1]		Line, load, temperature	4.85		5.15	V
Long-term Stability[1]		Over 1,000 hrs at 25° C		5	25	mV
Output Noise Voltage	V_{NOISE}	$10 \text{ Hz} \le f \le 100$ kHz, T_J = 25° C		50		µV
Short Circuit Current	I_{SC}		30	100	180	mA

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (-40 to 85° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{CC} = 15$ V, $R_T = 10$ kΩ, and $C_T = 3.3$ nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5 V Regulator						
Output Voltage	V_{REG}	$T_J = 25°$ C, $I_{REG} = 1$ mA	4.95	5.00	5.05	V
Line Regulation	PSRR	$12 \leq V_{CC} \leq 25$ V		2	10	mV
Load Regulation		$1 \leq I_{REG} \leq 20$ mA		2	10	mV
Temperature Stability[1]	TC_{REG}			0.2	0.4	mV/°C
Total Output Variation[1]		Line, load, temperature	4.85		5.15	V
Long-term Stability[1]		Over 1,000 hrs at 25° C		5	25	mV
Output Noise Voltage	V_{NOISE}	10 Hz $\leq f \leq$ 100 kHz, $T_J = 25°$ C		50		µV
Short Circuit Current	I_{SC}		30	100	180	mA
2.5 V Internal Reference						
5Nominal Voltage	V_{FB}	$T = 25°$ C; $I_{REG} = 1$ mA	2.470	2.500	2.535	V
Line Regulation	PSRR	12 V $\leq V_{CC} \leq 25$ V		2	5	mV
Load Regulation		$1 \leq I_{REG} \leq 20$ mA		2	5	mV
Temperature Stability[1]	TC_{VFB}			0.1	0.2	mV/°C
Total Output Variation[1]		Line, load, temperature	2.450	2.500	2.550	V
Long-term Stability[1]		Over 1,000 hrs at 125° C		2	12	mV
Oscillator						
Initial Accuracy	f_{OSC}	$T_J = 25°$ C	47	52	57	kHz
Voltage Stability		12 V $\leq V_{CC} \leq 25$ V		0.2	1	%
Temperature Stability[1]	TC_f	$T_{MIN} \leq T_J \leq T_{MAX}$		5		%
Amplitude	f_{OSC}	$V_{RT/CT}$ peak-to-peak		1.6		V
Upper Trip Point	V_H			2.9		V
Lower Trip Point	V_L			1.3		V
Discharge Current	I_D		7.5	8.7	9.5	mA
Duty Cycle Limit		$R_T = 680$ Ω, $C_T = 5.3$ nF, $T_J = 25°$ C	46	50	52	%

PRELIMINARY

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (-40 to 85° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error Amplifier						
Input Voltage	V_{FB}	T_J = 25° C	2.470	2.50	2.535	V
Input Bias Current	I_{BIAS}			–0.1	–1	µA
Voltage Gain	A_{VOL}	$2 \leq V_{COMP} \leq 4$ V	65	90	1	dB
Transconductance	G_m			1		mA/mV
Unity Gain Bandwidth[1]	GBW		0.8	1.2		MHz
Power Supply Rejection Ratio	PSRR	$12 \leq V_{CC} \leq 25$ V	60	70		dB
Output Sink Current	I_{COMPL}	V_{FB} = 2.7 V, V_{COMP} = 1.1V	2	6		mA
Output Source Current	I_{COMPH}	V_{FB} = 2.3 V, V_{COMP} = 5 V	0.5	0.8		mA
Output Swing High	V_{COMPH}	V_{FB} = 2.3 V, R_L = 15 kΩ to Ground	5	5.5		V
Output Swing Low	V_{COMPL}	V_{FB} = 2.7 V, R_L = 15 kΩ to Pin 8		0.7	1.1	V
Current Sense Comparator						
Transfer Gain[2,3]	AV_{CS}	$-0.2 \leq V_{SENSE} \leq 0.8$ V	2.85	3.0	3.15	V/V
I_{SENSE} Level Shift[2]	V_{LS}	V_{SENSE} = 0 V		1.5		V
Maximum Input Signal[2]		V_{COMP} = 5 V	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	$12 \leq V_{CC} \leq 25$ V		70		dB
Input Bias Current	I_{BIAS}			–1	–10	µA
Propagation Delay to Output[1]	t_{PD}			150	300	ns
Output						
Output Low Level	V_{OL}	I_{SINK} = 20 mA		0.1	0.4	V
	V_{OL}	I_{SINK} = 200 mA		1.5	2.2	V
Output High Level	V_{OH}	I_{SOURCE} = 20mA	13	13.5		V
	V_{OH}	I_{SOURCE} = 200mA	12	13.5		V
Rise Time[1]	t_R	C_L = 1 nF		50	150	ns
Fall Time[1]	t_F	C_L = 1 nF		50	150	ns
Housekeeping						
Start-up Threshold	VCC(on)	3842/4	15	16	17	V
		3843/5	7.8	8.4	9.0	V
Minimum Operating Voltage After Turn On	VCC(min)	3842/4	9	10	11	V
		3843/5	7.0	7.6	8.2	V
Output Low Level in UV State	V_{OUV}	I_{SINK} = 20 mA, V_{CC} = 6 V		1.5	2.0	V
Over-Temperature Shutdown[4]	T_{OT}			125		°C

PRELIMINARY

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (-40 to 85° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PWM						
Maximum Duty Cycle Minimum Duty Cycle	D_{max} D_{min}	**3842/3** 3842/3	**94**	**97**	**100** 0	**%** %
Maximum Duty Cycle	D_{max}	3844/5	49	49.5	50	%
Minimum Duty Cycle	D_{min}	3844/5			0	%
Supply Current						
Start-up Current	I_{CC}	3842/4, $V_{FB} = V_{SENSE} = 0$ V, V_{CC} = 14 V		0.5	1.0	mA
		3843/5, $V_{FB} = V_{SENSE} = 0$ V, V_{CC} = 7 V		0.3	0.5	mA
Operating Supply Current	I_{CC}			9	17	mA
V_{CC} Zener Voltage	V_Z	I_{CC} - 25 mA		30		V

Notes:

1. This parameter is not 100% tested in production.
2. Parameter measured at trip point of PWM latch.
3. Transfer gain is the relationship between current sense input and corresponding error amplifier output at the PWM latch trip point and is mathematically expressed as follows:

$$A = \frac{\Delta I_{COMP}}{\Delta V_{SENSE}}; -0.2 \le V_{SENSE} \le 0.8\ V$$

4. At the over-temperature threshold, TOT, the oscillator is disabled. The 5 V reference and the PWM stages, including the PWM llatch, remain powered.

PRELIMINARY

Typical Performance Curves

Supply Current vs Supply Voltage

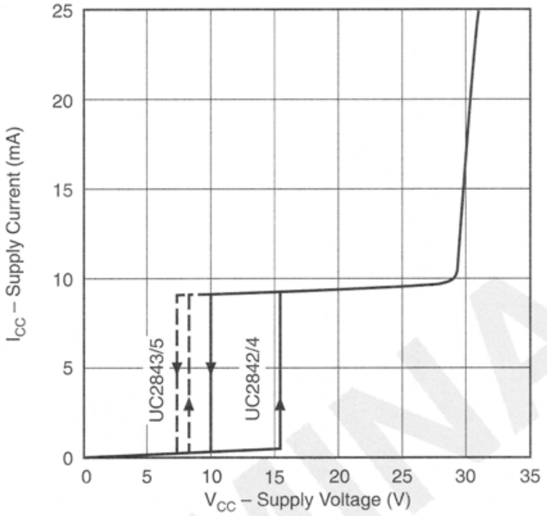


Figure 2

Regulator Output Voltage vs Ambient Temperature

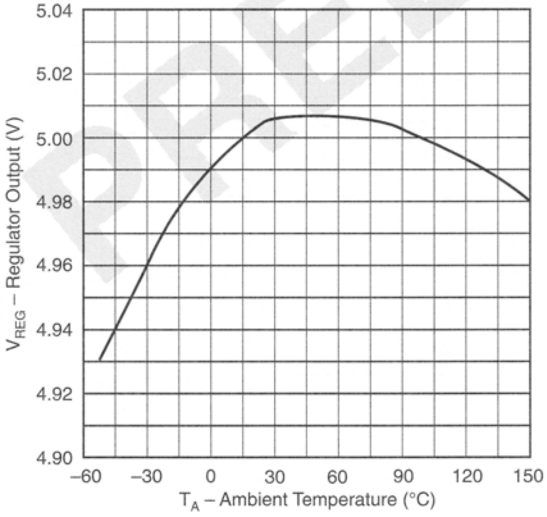


Figure 3

Regulator Short Circuit Current vs Ambient Temperature

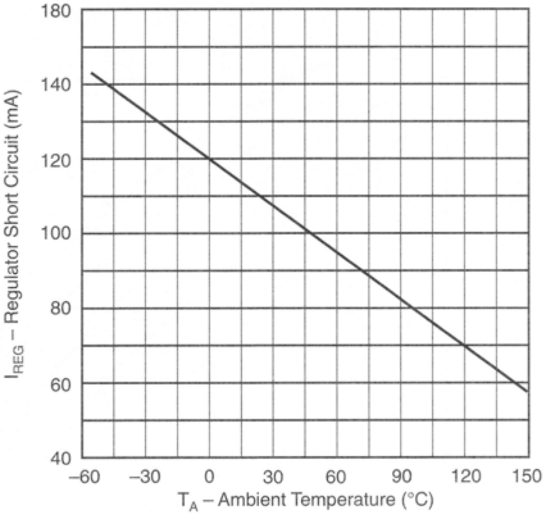


Figure 4

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Typical Performance Curves

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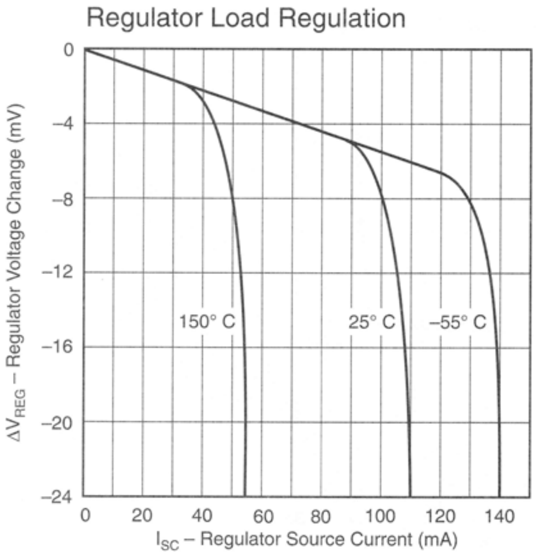
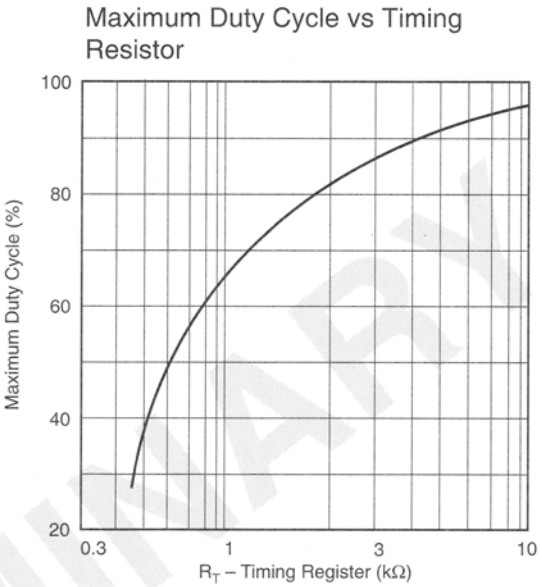


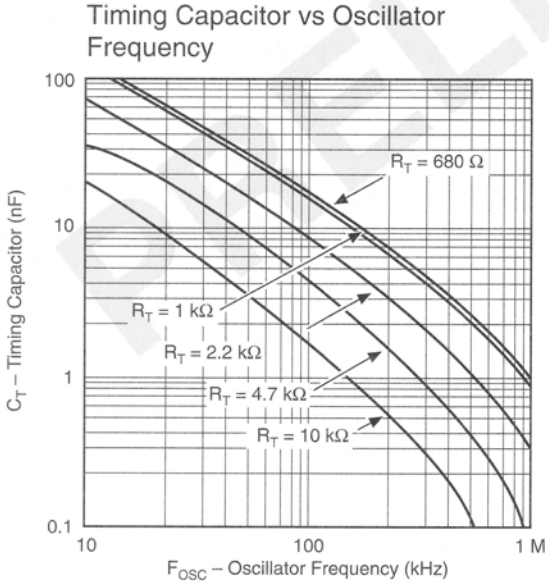
Regulator Load Regulation

Figure 5



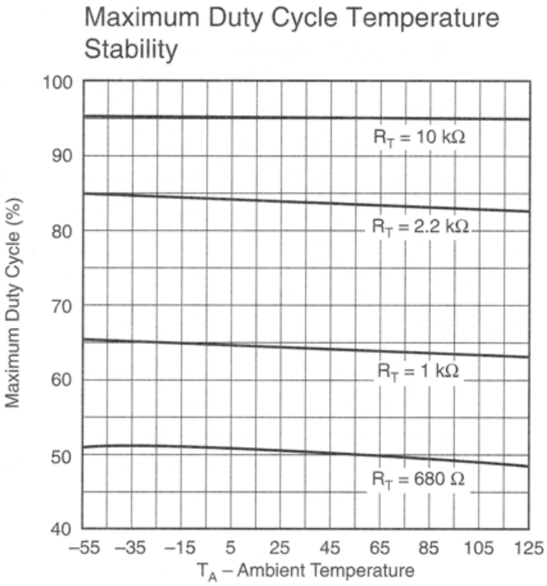
Maximum Duty Cycle vs Timing Resistor

Figure 6



Timing Capacitor vs Oscillator Frequency

Figure 7



Maximum Duty Cycle Temperature Stability

Figure 8

Typical Performance Curves

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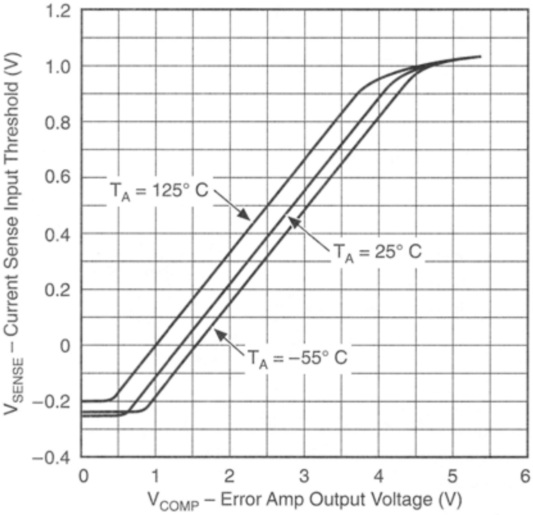

Current Sense Input Threshold vs Error Amp Output Voltage

Figure 9

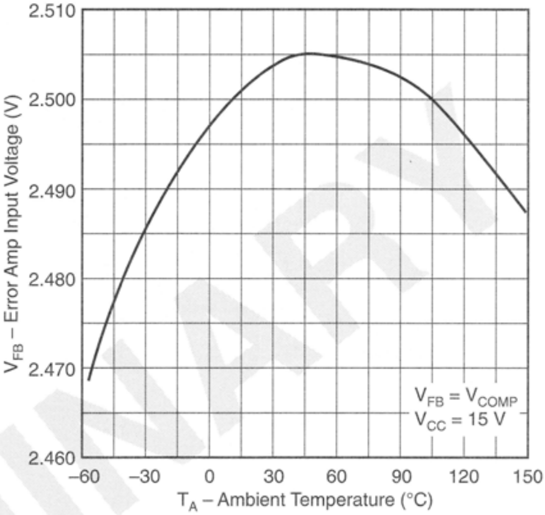

Error Amp Input Voltage vs Ambient Temperature

Figure 10

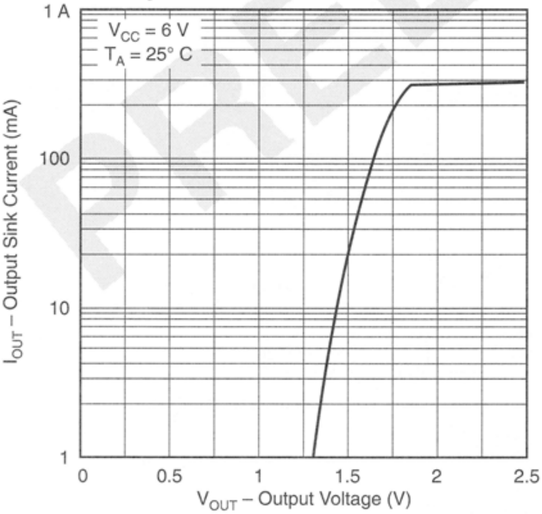

Output Sink Capability In Under-Voltage Mode

Figure 11

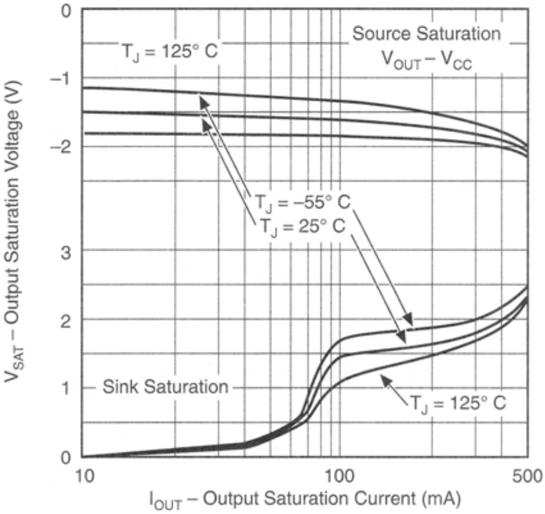
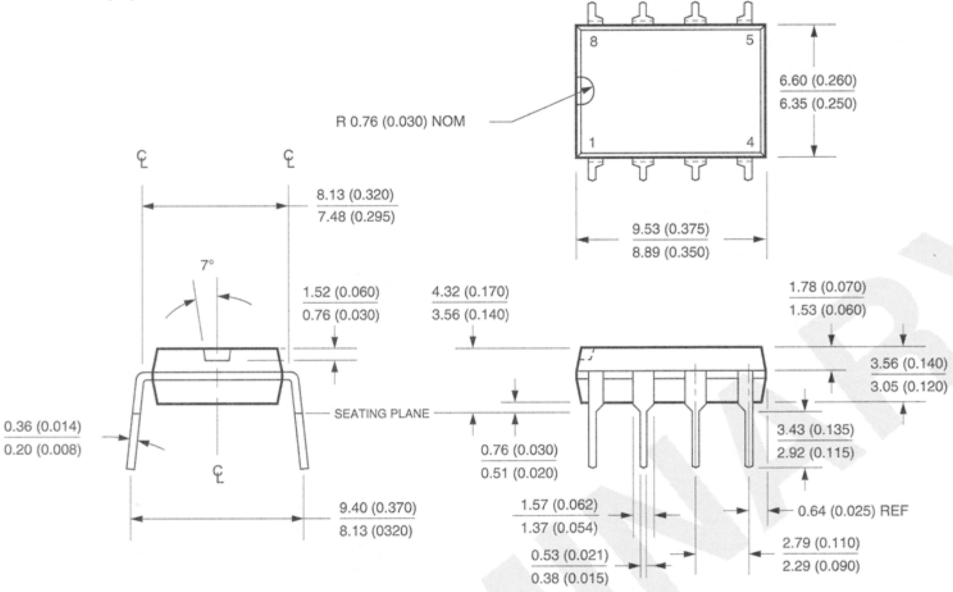

Output Saturation Voltage

Figure 12

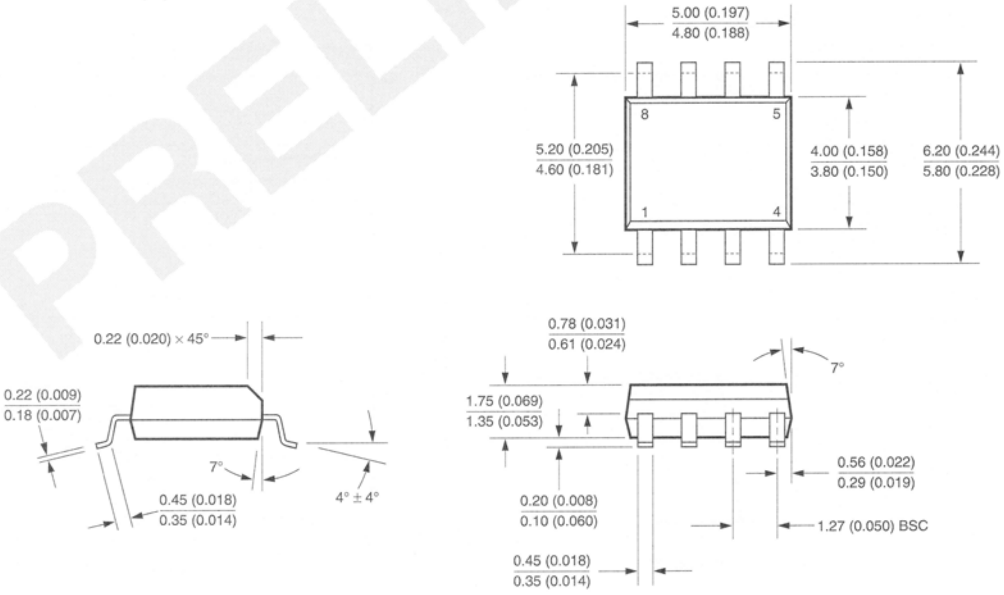
Package Dimensions

All Dimensions in mm (Inches)

8-Pin Plastic DIP (N)



8-Pin Plastic SOIC (D)



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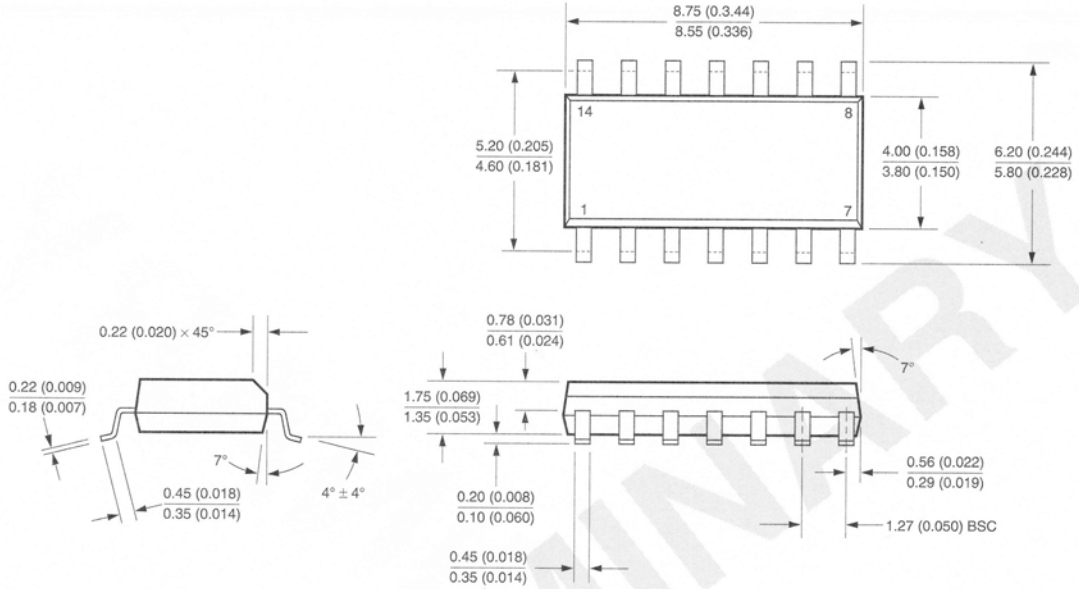
Package Dimensions

All Dimensions in mm (Inches)

14-Pin Plastic SOIC (D)



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ASTEC SEMICONDUCTOR

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Notes

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UC3842/3/4/5

Current Mode Controller

Preliminary Specification

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Features

- 2.5 V bandgap reference trimmed to 1% and temperature compensated
- UC3842/3 oscillators trimmed for precision duty cycle clamp
- Improved specs on UVLO and hysteresis provide more predictable start-up and shut-down
- Improved 5 V regulator provides better AC noise immunity
- Guaranteed performance with I_{SENSE} pulled below ground
- Over-temperature shutdown
- Current mode operation to 500 kHz
- Low start-up and operating current
- Low cost

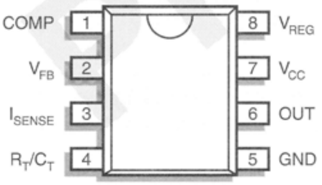
Description

The UC3842/3/4/5 family of control IC's are fixed frequency current mode pulse width modulation controllers. They provide all the features necessary to implement off-line or DC to DC convertor applications with a minimal number of external components.These circuits include a precision bandgap reference trimmed for 1% accuracy at the error amp input, a trimmed oscillator discharge current for precise maximum duty cycle control, a high gain error amplifier, a PWM comparator providing cycle-by-cycle current limit control and a high current totem pole output for driving power MOSFETs.

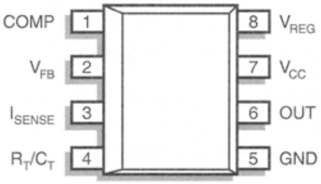
The UC3842 and UC3844 have under-voltage lockout thresholds of 16V (on) and 10V (off), making them ideal for off-line applications. The UC3843 and UC3845 have UVLO thresholds of 8.4V (on) and 7.6V (off), and require less than 0.5 mA of startup current. The UC3842 and UC3843 operates at duty cycles near 100%. The UC3844/45 have a maximum duty cycle range from 0% to 50%, due to an internal flip-flop that blanks the output at every other clock cycle.

Pin Configuration — Top view

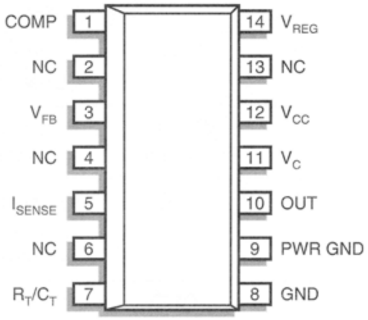
PDIP (N)



8L SOIC (D)



14L SOIC (D)



Ordering Information

Description	Temperature Range	Order Codes
8-Pin Plastic DIP	0 to 70° C	UC3842/3/4/5N
8-Pin Plastic SOIC	0 to 70° C	UC3842/3/4/5D-8
14-Pin Plastic SOIC	0 to 70° C	UC3842/3/4/5D-14

Functional Block Diagram

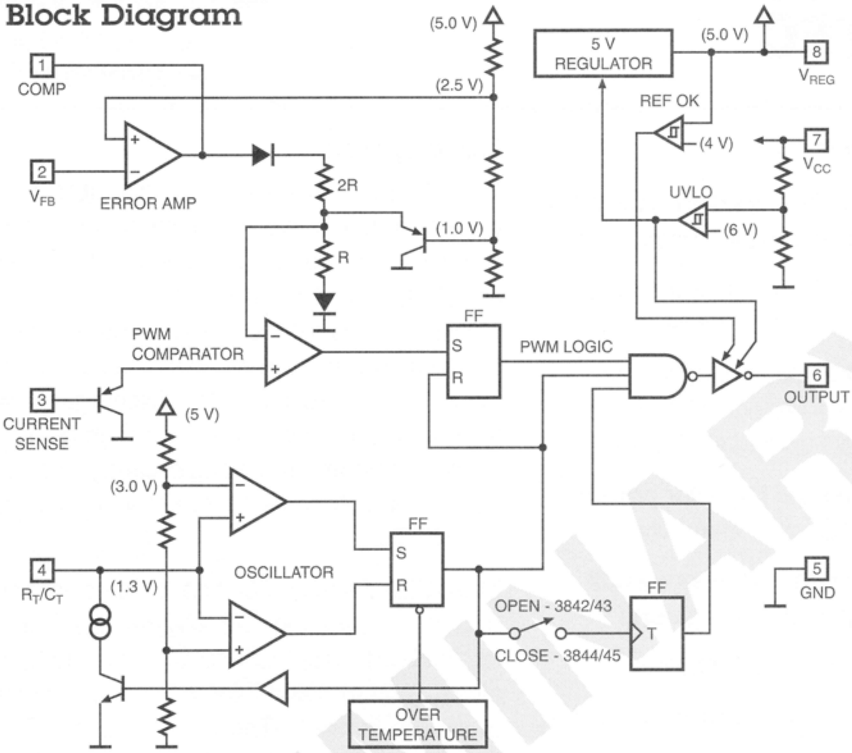


Figure 1. Block Diagram of the UC3842/3/4/5

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Pin Function Description

Pin Number	Function	Description
1	COMP	This pin is the error amplifier output. Typically used to provide loop compensation to maintain V_{FB} at 2.5 V.
2	V_{FB}	Inverting input of the error amplifier. The non-inverting input is a trimmed 2.5 V bandgap reference.
3	Current Sense	A voltage proportional to inductor current is connected to the input. The PWM uses this information to terminate the gate drive of the output.
4	R_T/C_T	Oscillator frequency and maximum output duty cycle are set by connecting a resistor (R_T) to V_{REG} and a capacitor (C_T) to ground. Pulling this pin to ground or to V_{REG} will accomplish a synchronization function.
5	GND	Circuit common ground, power ground, and IC substrate.
6	Output	This output is designed to directly drive a power MOSFET switch. This output can sink or source peak currents up to 1A. The output for the UC3844/5 switches at one-half the oscillator frequency.
7	V_{CC}	Positive supply voltage for the IC.
8	V_{REG}	This 5 V regulated output provides charging current for the capacitor C_T through the resistor R_T.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage (I_{CC} < 30 mA)	V_{CC}	Self-Limiting	V
Supply Voltage (Low Impedance Source)	V_{CC}	30	V
Output Current	I_{OUT}	±1	A
Output Energy (Capacitive Load)		5	µJ
Analog Inputs (Pin 2, Pin 3)		−0.3 to 30	V
Error Amp Sink Current		10	mA
Maximum Power Dissipation	P_D		
8L SOIC		750	mW
8L PDIP		1000	mW
14L SOIC		950	mW
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}		
UC3842,4		15	V
UC3843,5		10	V
Oscillator	f_{OSC}	50 to 500	kHz

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
8L PDIP	95° C/W	50° C/W	10.5 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C
14L SOIC	130° C/W	35° C/W	7.7 mW/°C

Electrical Characteristics

Electrical characteristics are guaranteed over full junction temperature range (0 to 70° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5 V Regulator						
Output Voltage	V_{REG}	T_J = 25° C, I_{REG} = 1 mA	4.95	5.00	5.05	V
Line Regulation	PSRR	$12 \leq V_{CC} \leq 25$ V		2	10	mV
Load Regulation		$1 \leq I_{REG} \leq 20$ mA		2	10	mV
Temperature Stability[1]	TC_{REG}			0.2	0.4	mV/°C
Total Output Variation[1]		Line, load, temperature	4.85		5.15	V
Long-term Stability[1]		Over 1,000 hrs at 25° C		5	25	mV
Output Noise Voltage	V_{NOISE}	$10 \text{ Hz} \leq f \leq 100$ kHz, T_J = 25° C		50		µV
Short Circuit Current	I_{SC}		30	100	180	mA

PRELIMINARY

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 70° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5 V Regulator						
Output Voltage	V_{REG}	T_J = 25° C, I_{REG} = 1 mA	4.95	5.00	5.05	V
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Load Regulation		$1 \le I_{REG} \le 20$ mA		2	10	mV
Temperature Stability[1]	TC_{REG}			0.2	0.4	mV/°C
Total Output Variation[1]		Line, load, temperature	4.85		5.15	V
Long-term Stability[1]		Over 1,000 hrs at 25° C		5	25	mV
Output Noise Voltage	V_{NOISE}	10 Hz $\le f \le$ 100 kHz, T_J = 25° C		50		µV
Short Circuit Current	I_{SC}		30	100	180	mA
2.5 V Internal Reference						
5Nominal Voltage	V_{FB}	T = 25° C; I_{REG} = 1 mA	2.475	2.500	2.525	V
Line Regulation	PSRR	12 V $\le V_{CC} \le$ 25 V		2	5	mV
Load Regulation		$1 \le I_{REG} \le 20$ mA		2	5	mV
Temperature Stability[1]	TC_{VFB}			0.1	0.2	mV/°C
Total Output Variation[1]		Line, load, temperature	2.450	2.500	2.550	V
Long-term Stability[1]		Over 1,000 hrs at 125° C		2	12	mV
Oscillator						
Initial Accuracy	f_{OSC}	T_J = 25° C	47	52	57	kHz
Voltage Stability		12 V $\le V_{CC} \le$ 25 V		0.2	1	%
Temperature Stability[1]	TC_f	$T_{MIN} \le T_J \le T_{MAX}$		5		%
Amplitude	f_{OSC}	$V_{RT/CT}$ peak-to-peak		1.6		V
Upper Trip Point	V_H			2.9		V
Lower Trip Point	V_L			1.3		V
Discharge Current	I_D		7.5	8.7	9.5	mA
Duty Cycle Limit		R_T = 680 Ω, C_T = 5.3 nF, T_J = 25° C	46	50	52	%

PRELIMINARY

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 70° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{CC} = 15$ V, $R_T = 10$ kΩ, and $C_T = 3.3$ nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error Amplifier						
Input Voltage	V_{FB}	$T_J = 25°$ C	2.475	2.50	2.525	V
Input Bias Current	I_{BIAS}			–0.1	–1	µA
Voltage Gain	A_{VOL}	$2 \leq V_{COMP} \leq 4$ V	65	90	1	dB
Transconductance	G_m			1		mA/mV
Unity Gain Bandwidth[1]	GBW		0.8	1.2		MHz
Power Supply Rejection Ratio	PSRR	$12 \leq V_{CC} \leq 25$ V	60	70		dB
Output Sink Current	I_{COMPL}	$V_{FB} = 2.7$ V, $V_{COMP} = 1.1$V	2	6		mA
Output Source Current	I_{COMPH}	$V_{FB} = 2.3$ V, $V_{COMP} = 5$ V	0.5	0.8		mA
Output Swing High	V_{COMPH}	$V_{FB} = 2.3$ V, $R_L = 15$ kΩ to Ground	5	5.5		V
Output Swing Low	V_{COMPL}	$V_{FB} = 2.7$ V, $R_L = 15$ kΩ to Pin 8		0.7	1.1	V
Current Sense Comparator						
Transfer Gain[2,3]	AV_{CS}	$-0.2 \leq V_{SENSE} \leq 0.8$ V	2.85	3.0	3.15	V/V
I_{SENSE} Level Shift[2]	V_{LS}	$V_{SENSE} = 0$ V		1.5		V
Maximum Input Signal[2]		$V_{COMP} = 5$ V	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	$12 \leq V_{CC} \leq 25$ V		70		dB
Input Bias Current	I_{BIAS}			–1	–10	µA
Propagation Delay to Output[1]	t_{PD}			150	300	ns
Output						
Output Low Level	V_{OL} V_{OL}	$I_{SINK} = 20$ mA $I_{SINK} = 200$ mA		0.1 1.5	0.4 2.2	V V
Output High Level	V_{OH} V_{OH}	$I_{SOURCE} = 20$mA $I_{SOURCE} = 200$mA	13 12	13.5 13.5		V V
Rise Time[1]	t_R	$C_L = 1$ nF		50	150	ns
Fall Time[1]	t_F	$C_L = 1$ nF		50	150	ns
Housekeeping						
Start-up Threshold	VCC(on)	3842/4 3843/5	15 7.8	16 8.4	17 9.0	V V
Minimum Operating Voltage After Turn On	VCC(min)	3842/4 3843/5	9 7.0	10 7.6	11 8.2	V V
Output Low Level in UV State	V_{OUV}	$I_{SINK} = 20$ mA, $V_{CC} = 6$ V		1.5	2.0	V
Over-Temperature Shutdown[4]	T_{OT}			125		°C

PRELIMINARY

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 70° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{CC} = 15$ V, $R_T = 10$ kΩ, and $C_T = 3.3$ nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PWM						
Maximum Duty Cycle	$\mathbf{D_{max}}$	**3842/3**	**94**	**97**	**100**	**%**
Minimum Duty Cycle	D_{min}	3842/3			0	%
Maximum Duty Cycle	D_{max}	3844/5	49	49.5	50	%
Minimum Duty Cycle	D_{min}	3844/5			0	%
Supply Current						
Start-up Current	I_{CC}	3842/4, $V_{FB} = V_{SENSE} = 0$ V, $V_{CC} = 14$ V		0.5	1.0	mA
		3843/5, $V_{FB} = V_{SENSE} = 0$ V, $V_{CC} = 7$ V		0.3	0.5	mA
Operating Supply Current	I_{CC}			9	17	mA
V_{CC} Zener Voltage	V_Z	I_{CC} - 25 mA		30		V

Notes:

1. This parameter is not 100% tested in production.
2. Parameter measured at trip point of PWM latch.
3. Transfer gain is the relationship between current sense input and corresponding error amplifier output at the PWM latch trip point and is mathematically expressed as follows:

$$A = \frac{\Delta I_{COMP}}{\Delta V_{SENSE}};\ -0.2 \le V_{SENSE} \le 0.8\ V$$

4. At the over-temperature threshold, TOT, the oscillator is disabled. The 5 V reference and the PWM stages, including the PWM llatch, remain powered.

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Typical Performance Curves

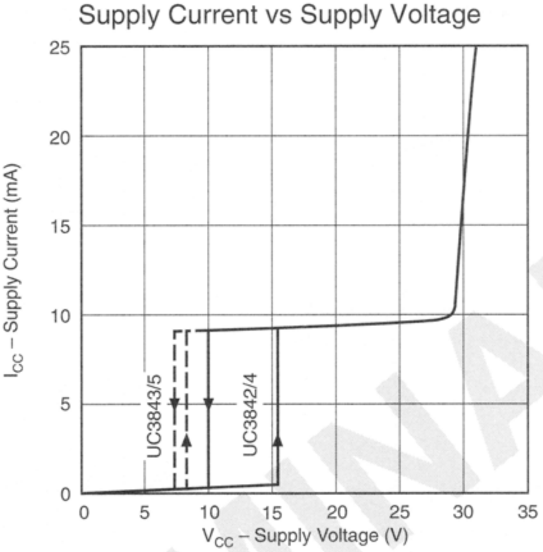


Figure 2

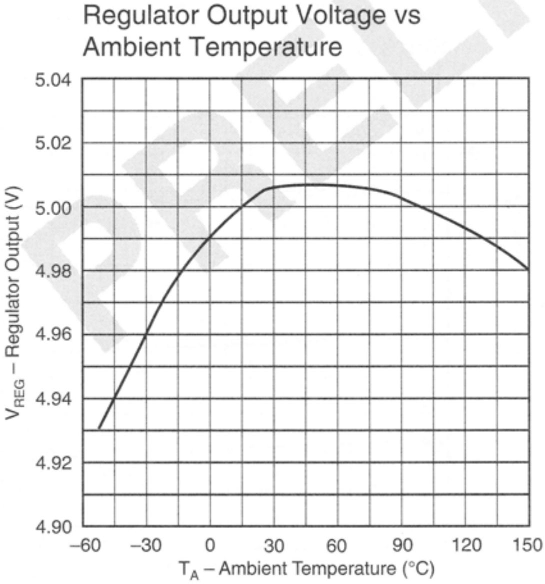


Figure 3

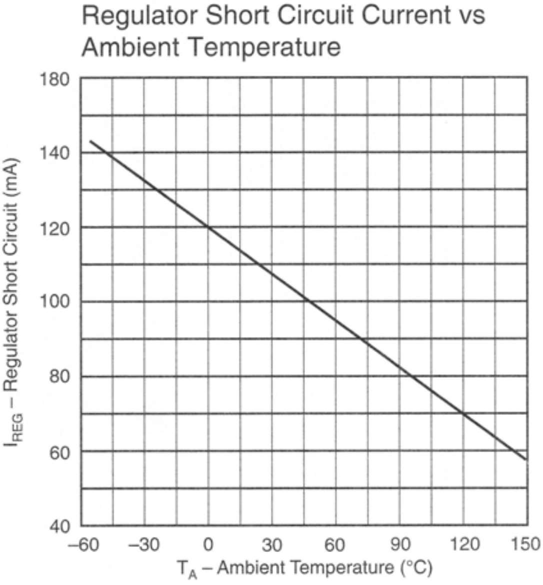


Figure 4

PRELIMINARY

Typical Performance Curves

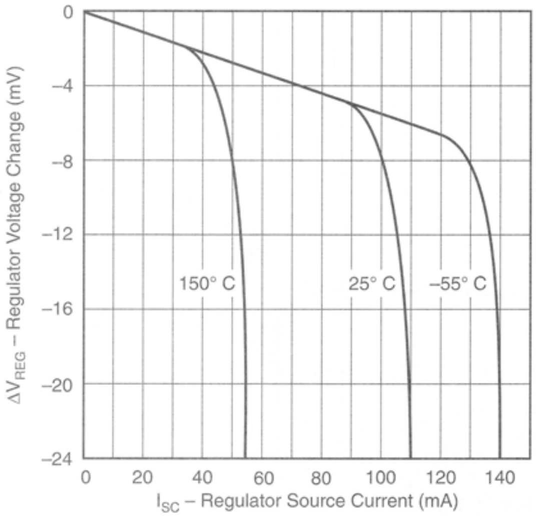

Regulator Load Regulation

Figure 5

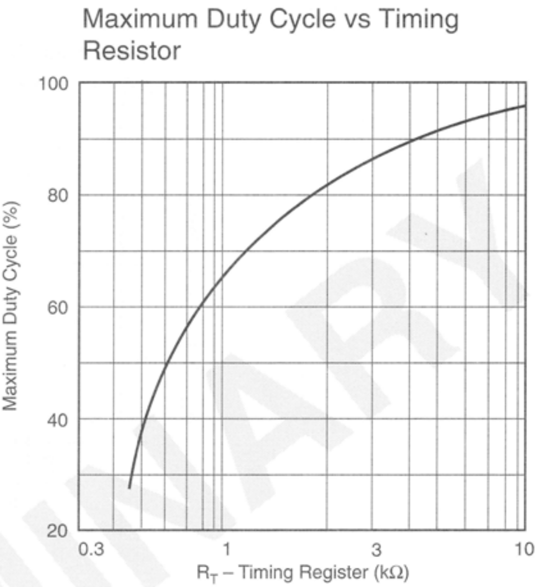

Maximum Duty Cycle vs Timing Resistor

Figure 6

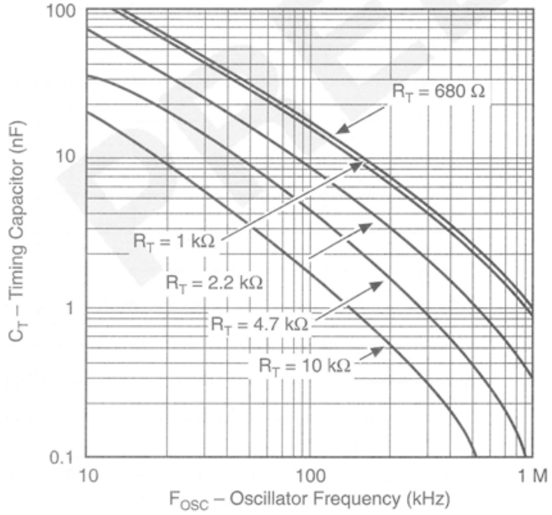

Timing Capacitor vs Oscillator Frequency

Figure 7

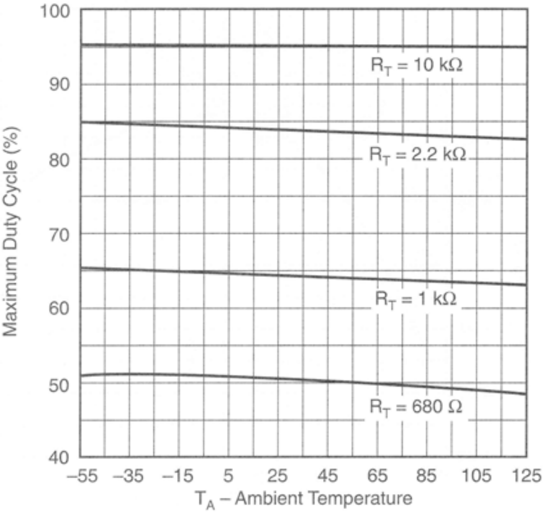

Maximum Duty Cycle Temperature Stability

Figure 8

PRELIMINARY

Typical Performance Curves

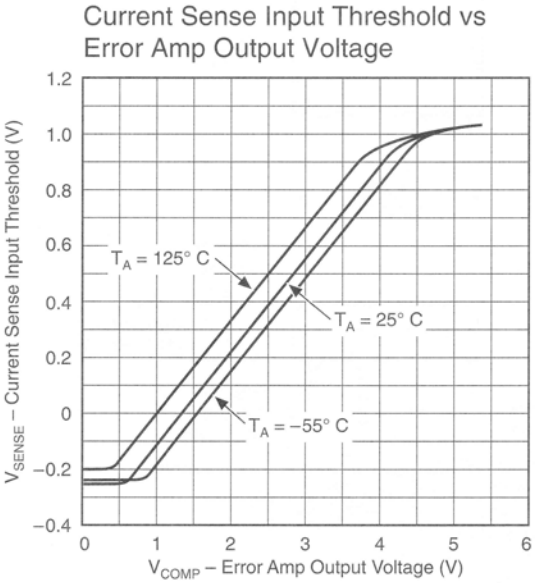


Figure 9

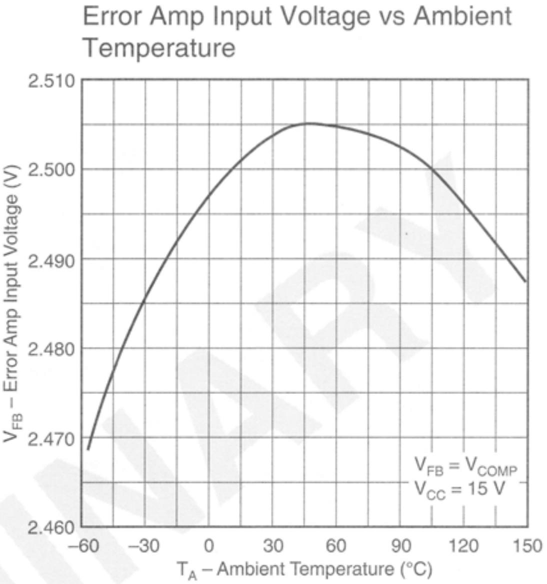


Figure 10

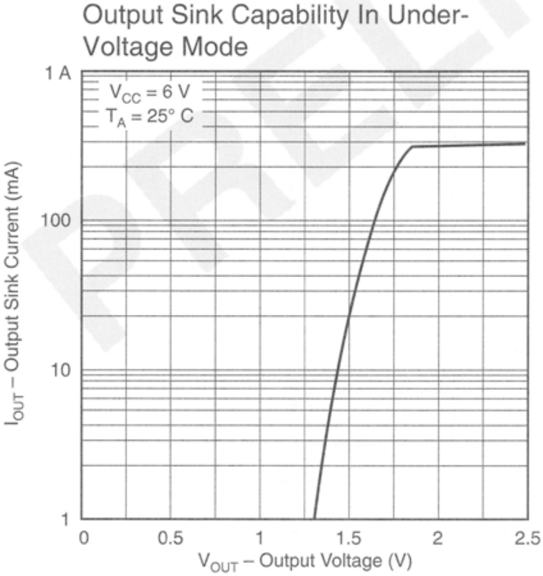


Figure 11

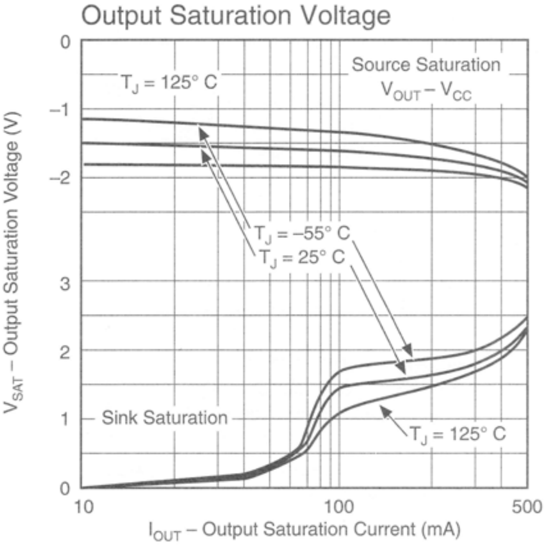


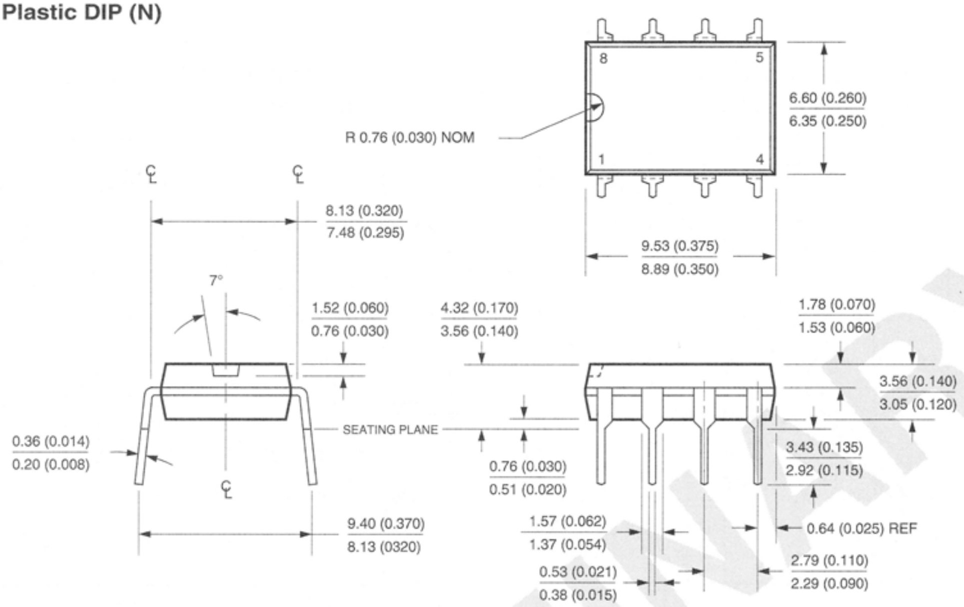
Figure 12

PRELIMINARY

Package Dimensions

All Dimensions in mm (Inches)

8-Pin Plastic DIP (N)



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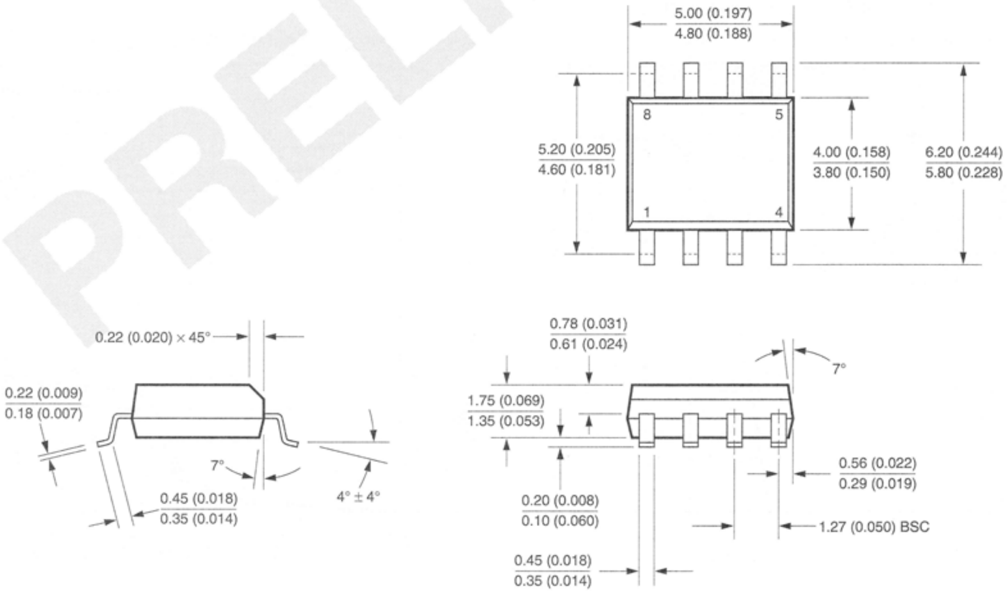
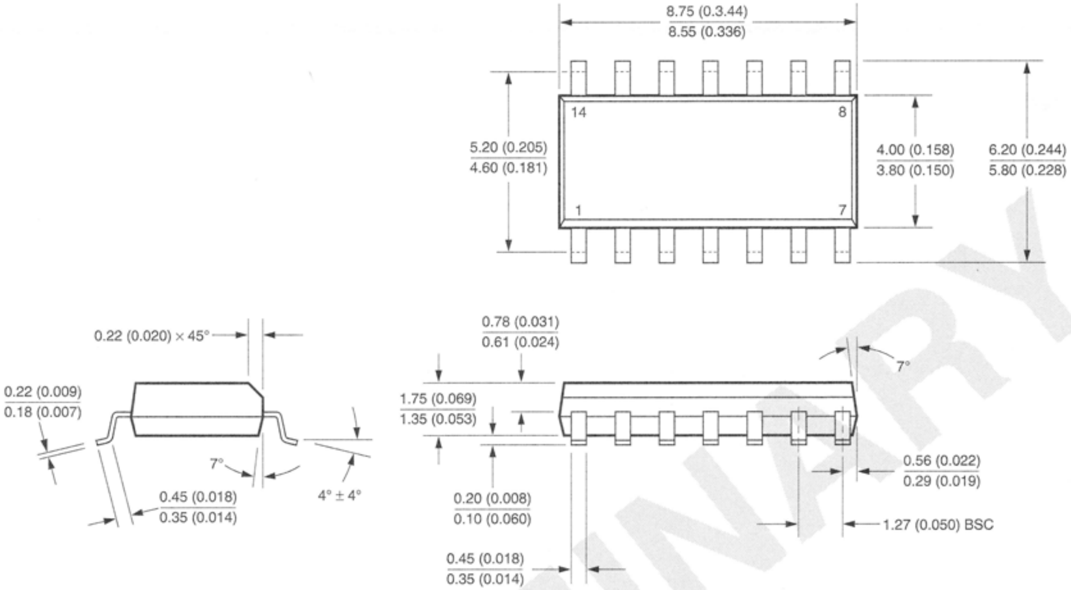
8-Pin Plastic SOIC (D)



Package Dimensions

All Dimensions in mm (Inches)

14-Pin Plastic SOIC (D)



PRELIMINARY

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Notes

ASTEC

AS384x/UC384x Compatibility Issues

Application Bulletin 1

While the Astec AS284x and the Astec UC384x and UC284x families of parts are generally equivalent functionally, the AS284x has both improved specifications and several features and capabilities not found on the UC284x series, nor in competitor's equivalent parts.

This bulletin is intended not to explain the specification differences such as tighter parameter distributions or wider temperature range. At issue, however, are the differences that might be seen in a given power supply when a UC384x is replaced by an AS384x, or vice versa. Where appropriate, differences between Astec UC384xs and other manufacturer's equivalents will be discussed as well.

Whether or not one part performs "better" is not always at question. What is at issue are differences that may make a power supply optimized with one family of parts non-optimal with the other. Although many of the minor differences appear only in unusual circumstances, designers must be able to predict when their "unconventional" design techniques may inadvertently expose a significant difference in the behavior of the control chip.

I. Reference

There is no difference between Astec AS284x and UC384x 5V regulators. There is, however, a difference between these parts and older versions of the AS3842. The latter part had a turn-on delay characterized by a slow ramp up to about 1.5V, followed by an abrupt turn-on. This problem is eliminated in the AS284x and UC384x series parts.

A difference exists between the start-up characteristic of the Astec parts compared with many competitors' parts. On many merchant market 384x chips, a turn-on overshoot is visible, which may reach 6V at its peak. This overshoot is usually very fast, typically less than half a volt, and is a function of load capacitance. The Astec part is much improved in this respect.

II. Oscillator

A. Frequency/ Duty Cycle Drift

There is a small oscillator drift over temperature that is common to all Astec parts but different than most competitive parts. The Astec part is optimized to provide a much improved duty cycle programming stability over temperature. This is at the expense of slightly higher frequency drift over temperature, though this drift is significantly smaller than allowed by specification. In typical applications, a drift in frequency is of much less concern than a varying maximum duty cycle.

B. Synchronization

Synchronization is generally not used in the power supplies typical of 384x designs, but the Astec AS284x parts are designed to transcend this low-cost/low performance distinction. An additional block of circuitry has been added to allow for external clocking and direct duty cycle control. This feature allows the use of an external digital clock that is in phase with the desired output. Our built-in clocking function makes driving the oscillator from an external logic source easier, but the addition of the low voltage sync threshold could cause incompatibility with some design techniques occasionally used with the UC384x.

Any circuit forcing the R_T/C_T pin to ground may behave differently when the AS284x is substituted for a UC series part. In particular, there are some methods of forcing a UC384x series part to synchronize to an external clock that may be problematic with an AS284x. When it is desired to synchronize using the lowest cost part, there are several schemes for synchronizing that perform equally well for both UC384x parts and for the AS284x. These schemes share a general requirement that the sync/oscillator waveform never drops below 1 V. These schemes are recommended as they allow the circuit design to migrate to an AS284x with a minimum of compatibility problems.

C. Very Low C_T Values

On our test jigs, we see occasional problems when trying to achieve high frequencies (>200 kHz) with very small capacitor values. Essentially, a small cap with a high value resistor can excite a poorly damped resonance using the inductance of the interconnect (or of the cap).

This is more a problem on the AS284x than the UC384x. If the resonant network rings below about .6V, it can trigger our sync circuit, causing some unusual behavior in the oscillator. As with most high frequency problems, careful layout and appropriate component selection are the solution to the problem. Several 500 kHz schemes, both with and without external clocks, have been successfully implemented. As a general rule, avoid R_T values in excess of 10k when using the AS284x unless the layout is well controlled.

III. Error Amplifier

A. Speed

The gain bandwidth of the op amp of the Astec parts is slightly higher than most competitor's parts (1.2 versus 1.0 MHz). Because of the use of junction capacitors as the compensation cap in the industry standard design, most competitive vendors' parts are far less controlled than Astec's (we use a cap with a glass dielectric and a metal top plate). In essense, we control our gain-bandwidth to be consistently where competitors occassionally find themselves with best-case parameter distributions.

B. Noise

Coming from a divider off of the 5V regulator, the internal 2.5V reference in the 3842 reflects the noise on that supply. Because of our improved regulator design and the use of ECL- type logic with low noise injection, there is far less noise on this reference point. Noise at this point effectively gets amplified to the COMP pin as a function of the external compensation network. Since any synchronous noise there effectively adds to or cancels some of the systems "slope" information, the rate of change of the noise at the time of the current sense amplifier switching event is a contributor to overall system gain.

Although it is arguable that no noise should be injected, the fact we have less noise is equivalent to having different noise, and may either improve or degrade a supply's loop stability (Certainly having less noise makes the system more predictable and less dependent on empirical tweaking).

C. Reference Accuracy

Although it may appear to be primarilly a specification issue, the AS284x has a significant improvement in the accuracy of the specification of the 2.5V reference at the V_{FB} input. Whereas the original designers of the UC3842 designed a 5V reference trimmed to 1% and then used a well matched divider to divide it down to 2.5V, ASD has found the original scheme to have unacceptable tolerances. Instead, all ASD parts are trimmed for 0.5% precision at the 2.5 V reference input, and all aditional tolerances are controlled to allow the 5V reference to remain within its usual specification for precision.

IV. Housekeeping

A. Turn-Off Behavior

Because of our multiple-redundant shut-off feature, ASD is currently seeing a benign but unexpected phenomenon at the turn-off threshold. If a noise-free DC supply is used to put the V_{CC} within about 10-30 mV of the threshold, as the part is about to shut off, there is an observed increase in the turn-on delay of the output stage. This is a result of the output blanking circuitry being prematurely turned on into a linear range as the UVLO comparator hits its threshold. The turn-off delay is not degraded, and therefore full control is maintained, but at a slightly reduced maximum duty cycle. This doesn't affect supply hold-up time, as this phenomenon happens only when in the region where supply shutdown is guaranteed.

C. Overtemp Shutdown

Unlike parts from other vendors, ASD limits the absolute maximum die temperature to about 135° C. This is done by disabling the oscillator. The 5V regulator, op amp, etc. remain biased on, as is the logic and output stage. Note: Since all circuits remain active after shutdown, but with a zero frequency oscillator, there can be an unusual waveform in DC testing. The output can go high during the final cycle, and awaits a termination signal from either the oscillator or the current sense amp. This may give the erroneous indication that the output "goes high" at shutdown. In fact, the PWM latch is still operative, and the normal termination of this cycle by the current sense comparator latches the output low until the overtemp condition is rectified. (Normally by the power being cycled, although if kept biased, the chip restarts after cooling down through a nominal temperature hysteresis band.)

V. Logic

A. Propagation Delay

From the current sense input to the output, the propagation delay in the AS284x is actually half the value of the UC384x (75–85 ns compared to 150–180 ns). This is arguably a great advantage, giving better control and significantly better protection from fault conditions, including core saturation. On the other hand, the AS284x comparator and logic sees a 50 ns noise spike as a significant event, whereas the UC384x may ignore it altogether.

Both the AS284x and UC384x series parts use common mode logic (ECL) for high speed, low noise injection, and process insensitivity. The difference in the parts lie in limiting the bandwidth of the comparator of the UC284x with a two stage nonlinear filter. This reduces noise sensitivity at the expense of some added propagation delay. The industry standard designs for the UC3842 family have similar propagation delays, but with those designs the delays are due to slow saturating RTL type logic and no effort is made to optimize the bandwidth of the current sense comparator.

B. AS2844/45 Flip-Flop Timing

The timing on the AS2844/5 is designed to guarantee a true 50% duty cycle, unlike the industry standard, which alternates simply both cycles and the oscillator discharge period.

We need to clarify, however, that the scheme actually guarantees less than 50% duty cycle. (50 kHz spec is 49% min, 50% max, actual is about 49.6%) There are asymmetrical logic delays in the system. In practice this causes the output pulse on the 3844 to be about 150 ns less than the expected 50%. This is a trivial error at 50 kHz, but at high frequencies it can become more of an issue. It is much more ideal than in the case of the UC3842 part, where the error is equal to the discharge time of the oscillator plus the delay asymmetries.

VI. I/O Clamping

A. Input Clamping Removed

The inputs of the error amplifier and current sense comparator (pins 2 and 3) are rugged epi-base diodes. These provide very high voltage breakdown (typically 60-80 V) and non-degrading performance under stress.The circuit design is such that no odd behavior occurs, even under extreme overvoltage conditions, and the absolute Maximum Ratings on these pins are Rated at 30 V. Several vendors have "protected" these inputs with low voltage (5.8 V) zeners to ground. With proper device design, these structures are not necessary and instead add a new source for leakage and parametric drift.

B. Comp Clamp

The error amp output on the UC3842 is nominally specified to have an output clamping action at 5 V minimum, 6 V typical. This clamping is typically accomplished with a 5.8 V zener. Instead, the Astec part clamps the error amp to one diode drop above VREG, or about 5.6V. This eliminates concern about zener leakage or drift and improves the ESD ruggedness of the circuitry.

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ASTEC

AS4301

Secondary Control Circuit

Features

- Error amp and reference emulate those of AS431
- Trimmed and temperature compensated 1% bandgap reference
- Use of AS4301 licenses ASTEC secondary control patent #4,323,961
- High 200 mA output current can directly drive pulse transformer
- Pulse transformer to primary provides feedback and isolation
- Inherent limiting of pulse width during start-up provides soft-start
- Inherent foldback current limiting
- Secondary ramp, derived from primary line voltage level, automatically improves power line transient rejection

Description

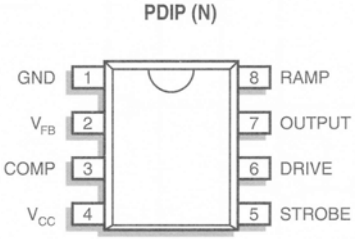
The AS4301 is a general purpose circuit for secondary control of isolated switch mode power supplies. The device contains a 2.5 V trimmed bandgap reference with a guaranteed 1% tolerance, a high gain inverting amplifier for use as an error amp, a comparator and a ramp generator for creating a pulse width modulator, and an output follower stage suitable for driving a coupling transformer to an isolated power stage.

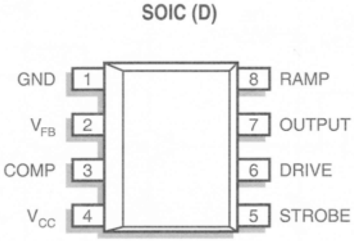
The secondary-based AS4301, unlike most PWM circuits, is intended to generate only the turn-off signal to end individual pulses initiated by separate primary based control circuit. Its general structure allows it to be used in both flyback and forward converters.

Ordering Information

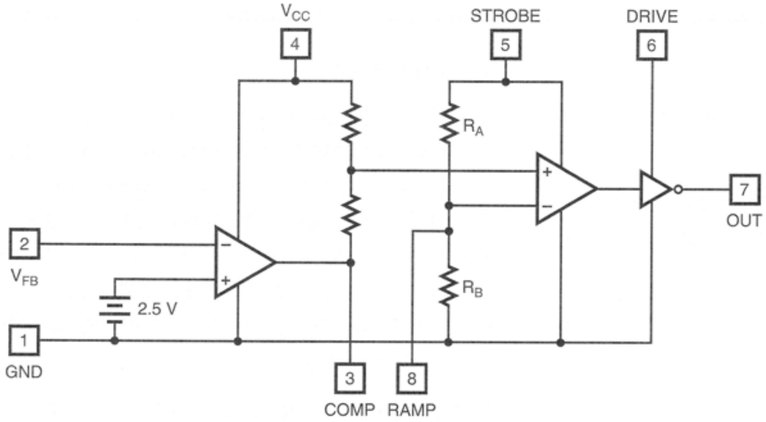
Description	Temperature Range	Order Codes
8-Pin Plastic DIP	0 to 105° C	AS4301N
8-Pin Plastic SOIC	0 to 105° C	AS4301D

Pin Configuration — Top view

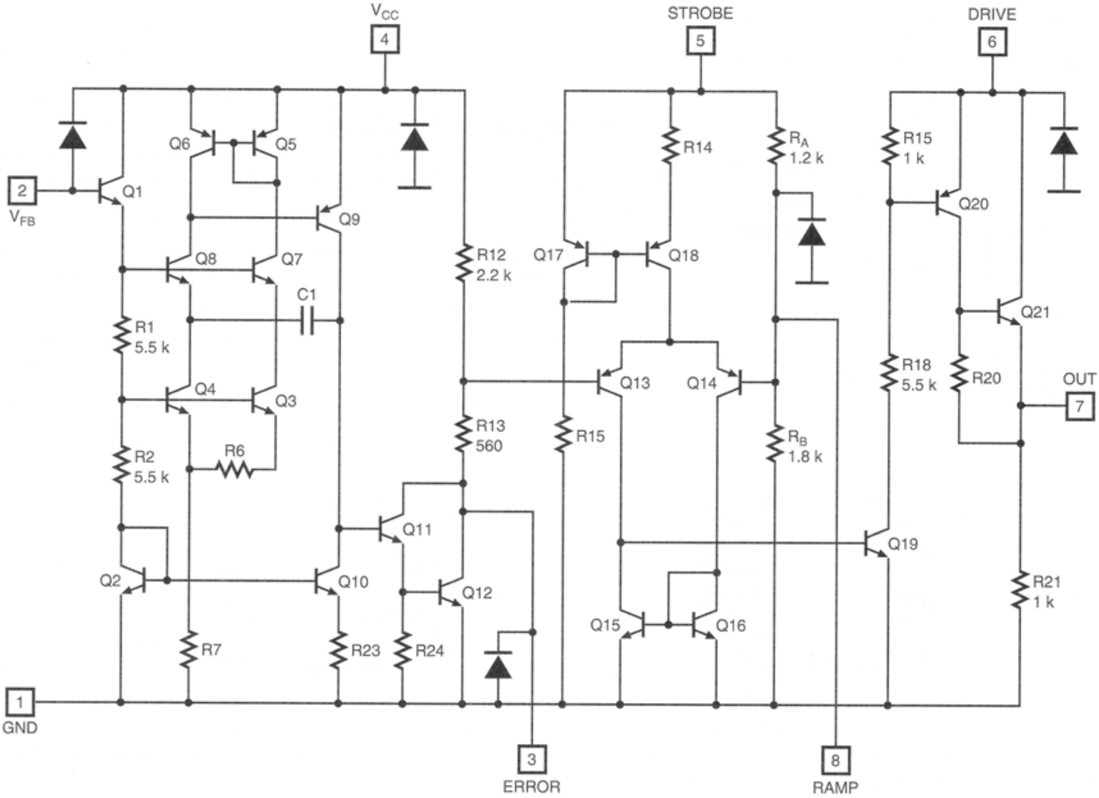




Functional Block Diagram



Simplified Schematic



Pin Function Description

Pin Number	Function	Description
1	GND	Circuit common ground and IC substrate. GND must be connected to the secondary ground for regulation.
2	V_{FB}	Inverting input of the error amplifier. The non-inverting input is a trimmed 2.5 V reference. This pin must not be pulled below –5 V and is clamped at $+V_{CC}$.
3	COMP	This error amplifier output is a collector of a Darlington NPN with a resistive pullup to V_{CC}. Typically used to provide loop compensation to maintain V_{FB} at 2.5 V. Clamped a diode drop below ground and should not exceed 10 mA in the clamped state.
4	V_{CC}	Supply voltage for the reference and error amplifier. This supply pin is typically tied to the regulated output of the power supply. Clamped a diode drop below ground and should not exceed 10 mA in the clamped state.
5	STROBE	Supply pin for the comparator and ramp generator. Typically tied to the secondary of the main power transformer, which may swing to negative voltage.
6	DRIVE	Supply pin for the output stage. This pin is also typically tied to the secondary of the power transformer with a series diode to prevent being pulled below ground. For reliable output, V_{DRV} must be between 6.4 and 35 V. Clamped a diode drop below ground and should not exceed 100 mA in the clamped state.
7	OUT	Output pulse is triggered high when ramp voltage exceeds the voltage at the error amplifier output. This pulse typically drives an isolation transformer to switch off the primary side power transistor. Upper clamp at V_{DRV} and lower clamp at a diode drop below ground, which should not exceed 200 mA.
8	RAMP	Connection for an external capacitor (typically 5 to 200 pF) for ramp generation with the internal voltage divider from V_{STROBE}. This line-dependent ramp sets the pulse width in conjunction with the internal comparator.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	36	V
Error Amplifier Output	V_{COMP}	36	V
Reference Input	V_{FB}	5	V
Strobe, Drive, Out, Ramp Input		46	V
Continuous Power Dissipation at 25° C	P_D		
8L PDIP		1000	mW
8L SOIC		750	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	2.9 to 20	V
Drive Voltage (pulsed)	V_{DRV}	6.5 to 35	V
Strobe (pulsed)	V_{STB}	−35 to 35	V
Operating Frequency	f_{OP}	10 to 400	kHz

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
8L PDIP	95° C/W	50° C/W	10.5 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C

Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{CC} = 8.5$ V and $I_{COMP} = 5$ mA unless otherwise stated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference/Amplifier						
Reference Voltage	V_{REF}	$T_A = 25°$ C	2.475	2.500	2.525	V
Temperature Deviation	ΔV_{REF}		−10	2	10	mV
Line Regulation	PSRR	$5\ V \leq V_{CC} \leq 20\ V$	−10	6.4	20	mV
Load Regulation		$1\ mA \leq I_{COMP} \leq 5\ mA$, $V_{COMP} = V_{REF}$	−20	−6.4	10	mV
Input Bias Current	I_{REF}	$T_A = 25°$ C		0.4	4	μA
Temperature Deviation	ΔI_{REF}			0.4	1.1	μA
Comp Output Voltage Low	$V_{COMP\ OL}$	$I_{COMP} = 8.5$ mA		0.8	3.0	V
Comp Sink Current	$I_{COMP\ OL}$	$V_{COMP} = 2.5$ V		170		mA
Open Loop Gain	A_{VOL}			55		dB
Gain Bandwidth Product	GBP	f = 1 MHz		30		MHz
Error Amp Slew Rate	SR	$V_{IN} = 250$ mV p-p, $C_L = 100$ pF		30		V/μS
PWM Comparator						
Propagation Delay to Output	t_{PD}			240		ns
R_A			0.83	1.10	1.70	kΩ
R_B			1.25	1.69	2.55	kΩ
Ratio	$R_B/(R_A + R_B)$		0.6	0.605	0.61	
Output						
Output Source Current	I_{OH}	$V_{OUT} = 0$ V, $V_{STB} = V_{DRV} = 12$ V	100	270	500	mA
		$V_{STB} = V_{DRV} = 6.5$ V	20	150	300	mA
Output Voltage High	V_{OH}	$I_{SOURCE} = 0$, $V_{STB} = V_{DRV} = 6.5$ V	5.25	5.6		V
		$I_{SOURCE} = 150$ mA, $V_{DRV} = 22$ V	17.5	19.7		V

Electrical Characteristics (cont'd)

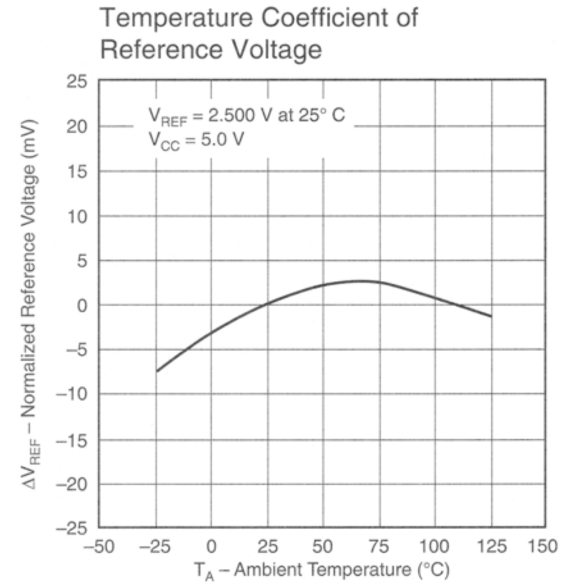
Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 8.5 V and I_{COMP} = 5 mA unless otherwise stated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage Low	V_{OL}	$V_{DRV} = 35$ V, $I_{SINK} = 0$		0.7	100	mV
Output Current Low	I_{OL}	$V_{DRV} = 30$ V		0.2	10	µA
Rise Time	t_R	$C_L = 100$ pF, $R_L = 1$ kΩ		60		ns
Maximum Drive Slew Rate[1]	dV/dt	Output transient peak ≤ 1.2 V	100	310		V/µS
Supply Current						
Strobe Current	I_{STB}	$V_{STB} = 30$ V	6	11	18	mA
		$V_{STB} = -30$ V	8	21	26.5	mA
$I_{CC} + I_{STB} + I_{DRV}$	I_{TOTAL}	$V_{CC} = V_{STB} = V_{DRV} = 12$ V				
		Output Off	2.5	4.6	7.5	mA
		Output On	12	25	36	mA
$I_{STB} + I_{DRV}$		$V_{STB} = V_{DRV} = 35$ V				
		Output Off	7.5	15	22.5	mA
		Output On	30	63	90	mA
$I_{STB} + I_{DRV}$[2]		$V_{STB} = V_{DRV} = 45$ V				
		Output Off	8	22.5	27	mA
		Output On	28	57	95	mA

Notes:

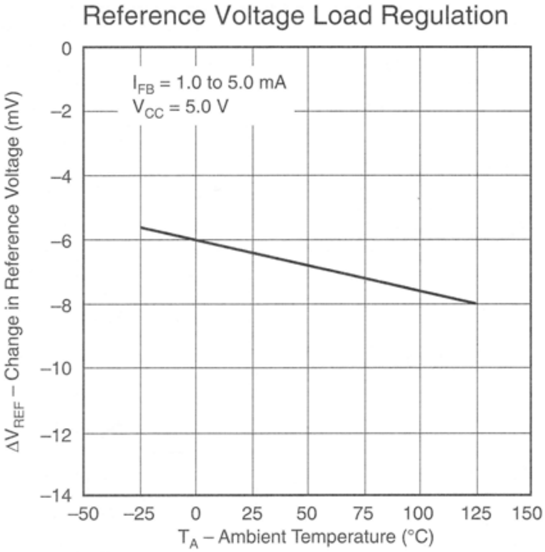
1. Drive supply is not to exceed minimum dV/dt or output may produce a transient spike.
2. $V_{STB} = V_{DRV} = 45$ V to simulate switching transients exceeding the 35 V maximum recommended operating condition.

Typical Performance Curves



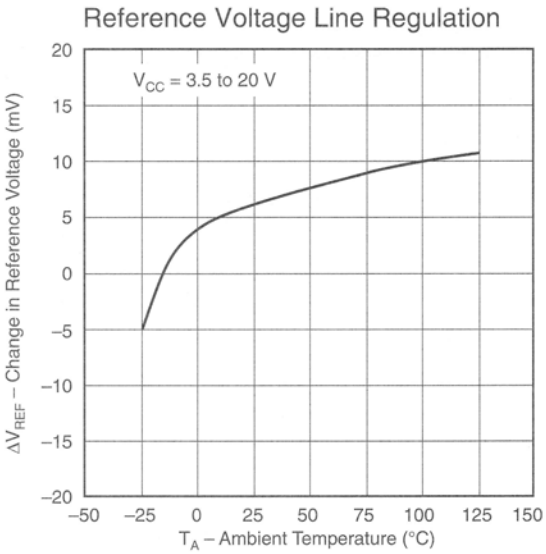
Temperature Coefficient of Reference Voltage

Figure 1



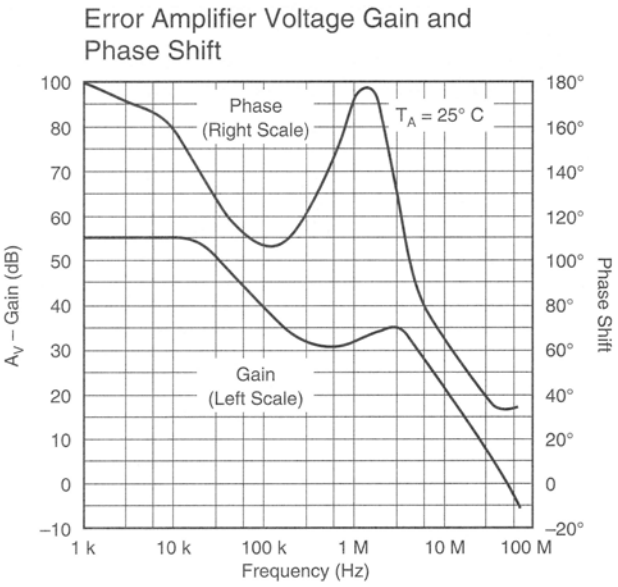
Reference Voltage Load Regulation

Figure 2



Reference Voltage Line Regulation

Figure 3



Error Amplifier Voltage Gain and Phase Shift

Figure 4

Typical Performance Curves

Dynamic Output Impedance of the Error Amplifier

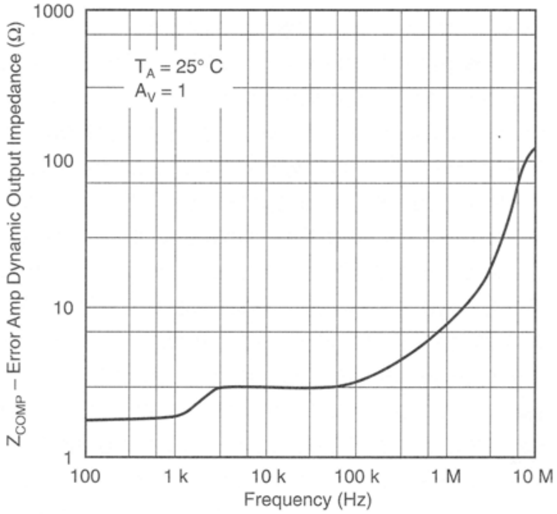


Figure 5

Power Supply Rejection Ratio of the Error Amplifier

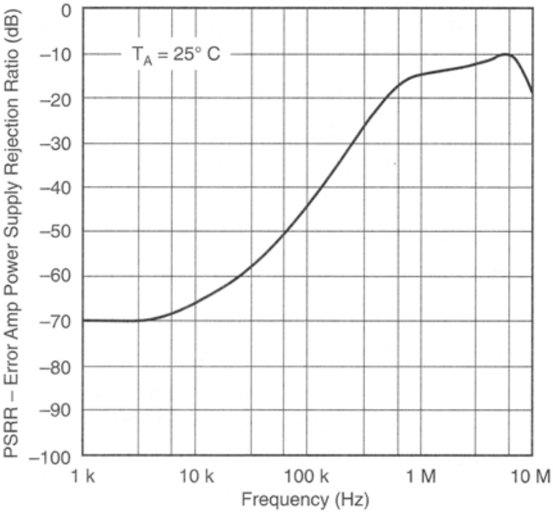


Figure 6

Strobe Current Characteristics

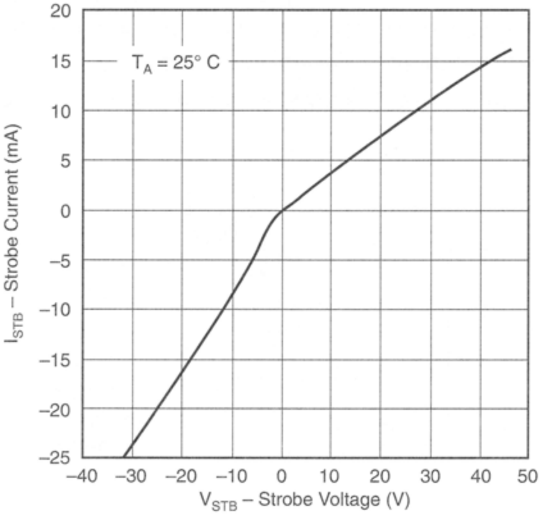


Figure 7

Output Saturation Voltage

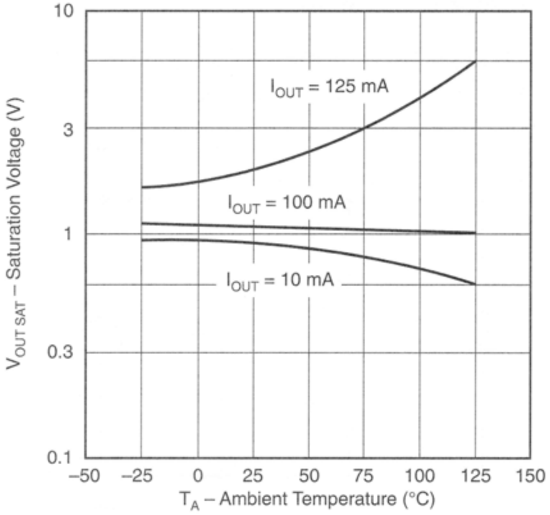


Figure 8

Theory of Operation

The AS4301 is a basic, yet powerful, secondary-based control circuit. It performs not only the essential function of the reference and error amplifier, but also the timing signal for terminating each cycle on a pulse-by-pulse basis. It communicates with a primary side power circuit via a simple pulse, which can be safety isolated magnetically or optically with minimal concern for the coupling system's waveform fidelity, linearity, or long-term drift. This allows for an inexpensive safety isolation without sacrificing system accuracy.

The AS4301 performs a basic volt-seconds control that is similar in concept to current mode control. Since the circuit regulates for a given volts-seconds product, it provides inherent rejection of input line changes, but without the necessity of directly sensing the switch current as with current mode controllers. And because the circuit provides an output indicating the time to turn off the power switch, it can be used in fixed or variable frequency supplies of almost any topology.

Flyback Operation

The operation of the AS4301 can be best described in terms of how it is used in a simple flyback power supply. Figure 9 shows the essential power circuit for such a supply, and the typical waveforms. To simplify the explanation, the assumption can be made that there is a 1:1 turns ratio in the transformer .

The transformer is used to store energy during t_{on}, the period when solid state switch SW1 is closed. The secondary circuitry will be disconnected by the reverse biased diode D1 during this period. Current will increase linearly with time based on the inductance of the primary winding of T1 and the applied voltage. When SW1 is opened, the stored energy in T1 causes the voltages on the windings to reverse (flyback), allowing D1 to conduct. The voltage across the transformer is clamped to the output voltage (assuming C_{OUT} is large) and the current in the secondary circuit decays linearly for period t_{fb}. The transformer then be resets and its voltage collapses. Depending on the control scheme, this may be a dwell period t_d during which no current flows in the transformer.

Two balance conditions are important in this supply at a given stable operating condition. First, there is an energy balance among stages. Neglecting minor power losses, the energy stored in the primary side inductance transfers to the output capacitor during the flyback interval. The

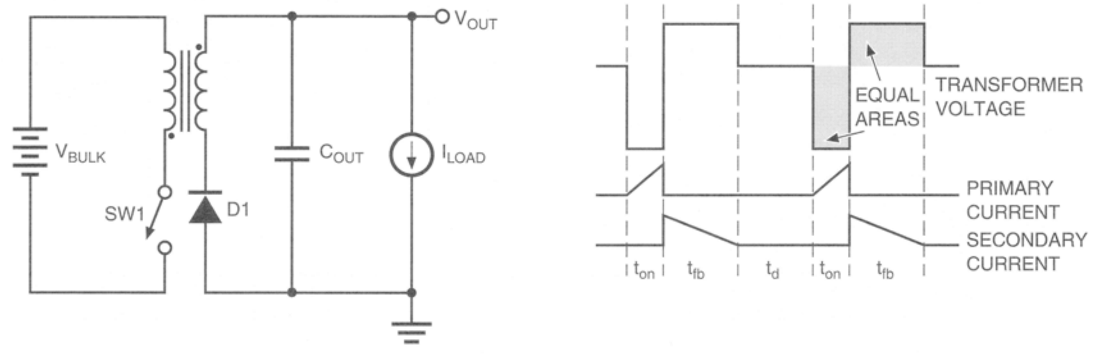


Figure 9. Simplified Flyback Circuit and Typical Waveform

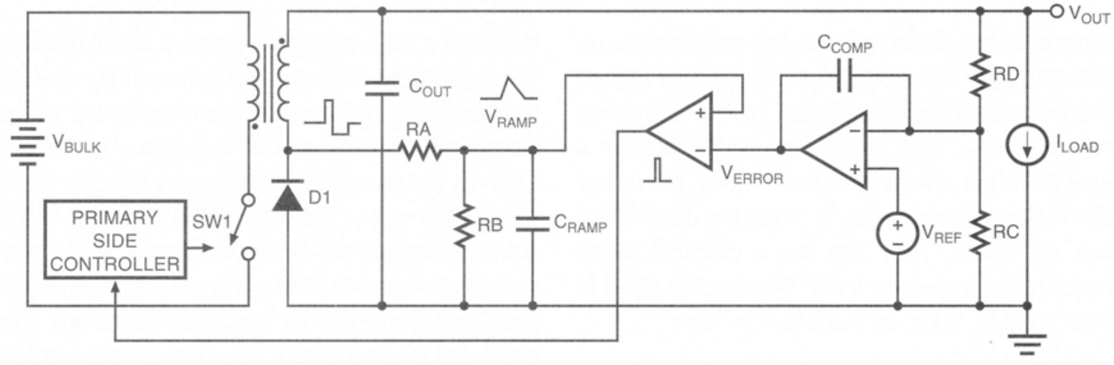


Figure 10. Secondary Controlled Flyback Power Supply

two energies balance, and are also equal to the net energy removed from the capacitor during each cycle by the load. Second, there needs to be a balancing of the V•t (volt-second) products on each winding, such that the net average drop across any winding is 0 Volts.

Flyback Control

Figure 10 shows the addition of three circuits that are used to determine the control of the power supply. On the right is the error amp and reference. These perform the normal function of reporting integrated loop error, with the secondary responsibility for providing frequency compensation for an overall feedback loop. By using a nearly infinite DC gain amplifier, the average output voltage can be regulated to almost arbitrary precision.

The second added circuit is the volt-second integrator on the left. Note that since there is no DC voltage across the secondary winding, the lower end of the transformer winding is at the same DC potential as V_{OUT}. The switching waveforms appearing on the primary winding also appear here. Integrating the AC component gives a measure of the V·t product currently applied to the winding. Although a single RC network could be used, the use of a resistive divider puts the output of the network at a fraction of the DC output voltage. Operation below V_{OUT} is useful since it allows active signal processing circuitry operating with V_{OUT} as a positive supply rail to have this signal, V_{RAMP}, well within its normal supply range.

In most pulse width control schemes, the error amp is compared with a ramp voltage to create a pulse train. In standard voltage mode (duty cycle programmed) modulators, the error amp would be compared with a fixed ramp oscillator. In current mode (peak current programmed) modulators, the error amp output is compared to a voltage that is a measure of instantaneous switch current. In this Volt-second programmed converter, the error amp is compared with V_{RAMP}, the ramp generated by the volt-second integrator, which, in the short-term, forces a fixed V•t product in the magnetics. The nature of a volt-second programmed system is such that if, for example input voltage is instantaneously increased, the pulse width is immediately reduced due to the steeper slope on the ramp signal. This will reject all input ripple open loop. Such open loop correction reduces the amount of overall feedback required for a given performance level.

A simple comparator, the third added circuit, connected to V_{RAMP} and V_{ERROR}, is used to generate a pulse that causes the switch to terminate its cycle. This allows for only a single signal, which determines the timing of the transition from t_{on} to t_{fb}. The secondary control scheme does not force an operating frequency, but rather allows the primary circuit to make the decision to turn on again. This can be a clocked (fixed frequency) turn on, or it can be synchronized to other events, such as transformer reset.

AS4301

One of the tricks involved in making secondary control work is developing a scheme to allow the control circuitry to function even in the absence of an output voltage (*eg.* start-up or shorted output.)

The AS4301 solves this problem by providing three supply voltage pins. V_{CC} is the supply rail for the error amp and is typically tied to the supply's output voltage. STROBE is the input to the volt-second integrator and comparator. Since the only time the comparator needs to function is during the period when the main power switch is on, this supply is usually taken directly from the transformer secondary. For generality, the STROBE input is made bipolar, able to tolerate connections swinging both positive and negative.

The DRIVE pin is the supply rail for the output stage. This output is an NPN voltage follower, swinging positive to terminate the cycle. Like the STROBE pin, it is needed only during t_{on}, so it is driven from the secondary winding. There are, however, two potential problems that must be avoided. Unlike the STROBE pin, the DRIVE pin cannot be driven negative, as it inherently clamps itself a diode drop below chip ground (substrate). An external diode is typically used to prevent reverse current flow from this pin. Second, the output stage has a finite signal feedthrough. Due to strictly capacitive effects, driving DRIVE positive with a step voltage creates a small glitch at the output pin. This can be reduced by slowing the rise time or lowering the impedance at the output pin. But above a certain rate of change in DRIVE, the capacitive effects can actually begin to turn the output stage on. This is similar to the dV/dt limitation on thyristors. Though this phenomenon is non-latching, it provides more output than can generally be ignored. Therefore, it is essential to keep the dV/dt on the drive pin below the specified limit.

One of the interesting considerations is the start-up and short circuit behavior of converters built with such a secondary control scheme. In general, as output voltage goes down, the error amp demands more volt-seconds, ie, longer pulse widths. This is done by raising the error amp output voltage. But as output voltage drops, there is a point where the error amp output cannot rise because it is biased from the output voltage. So as the output voltage drops further, the effective volt-seconds demanded is reduced, giving a fold-back sort of current limiting. When the output is completely shorted or is 0 V at start-up, the secondary controller demands an end of cycle immediately, limited only by rise time and propagation delays. This minimum pulse width provides enough energy to start up the supply, but reduces stress in the short circuit condition.

A typical secondary circuit for a flyback and forward are shown in Figures 11 and 12. Note that DRIVE and STROBE are connected to the secondary winding, while V_{CC} is tied to the supply output. The RAMP pin, the divider for the volt-time integrator, has a capacitor to ground. The addition of a series resistor allows a small voltage step that gives improved performance at light load. The error amp is connected to a divider from the output and is connected essentially as an integrator. In addition to adding pole-zero

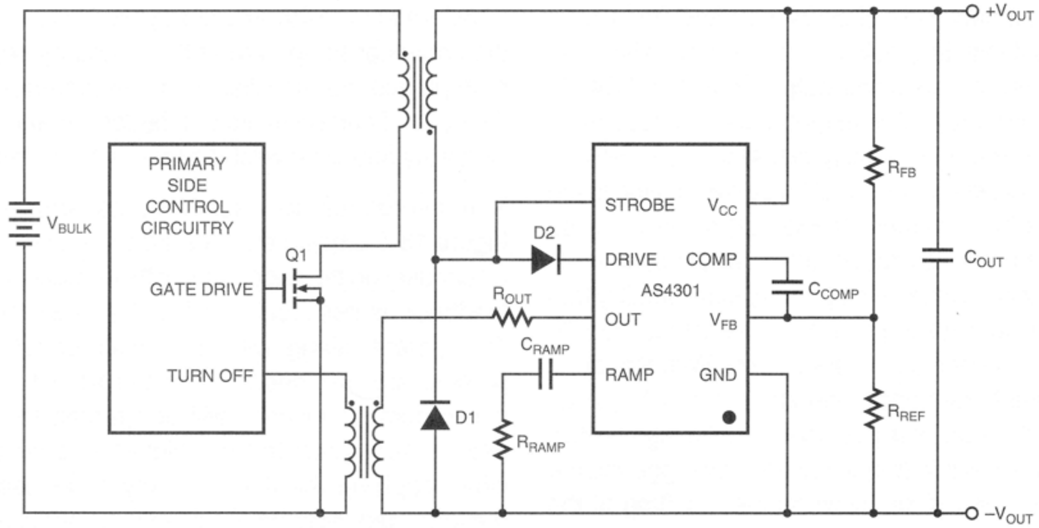


Figure 11. Secondary Controlled Flyback Power Supply Implementing the AS4301

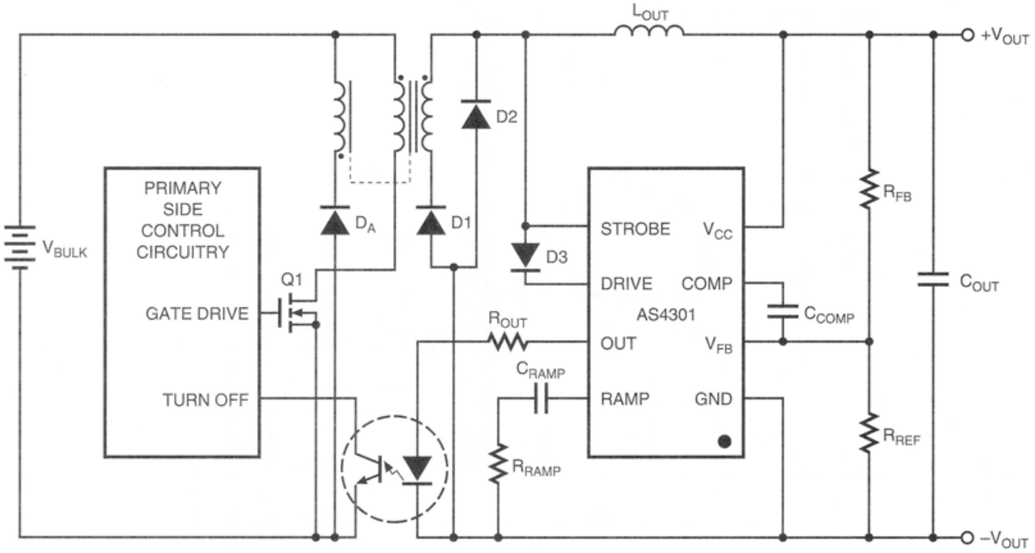


Figure 12. Secondary Controlled Forward Converter Implementing the AS4301

networks in the feedback path, there can be additional compensation networks added to the voltage divider, as indicated in the flyback example. The output can drive a transformer or an optocoupler, as indicated. Some series limiting resistance is useful, even with the transformer coupling scheme if the primary inductance is low or if the core is allowed to saturate.

The primary side circuitry has few limitations. It must initiate a pulse on the power switch and be able to detect the output from the AS4301 and terminate the output pulse in response. In general, it is usually advisable to provide a primary side current limit for power limiting in the case of a major fault. An example of this would be transformer saturation, which would cause significant currents in the primary side circuitry that would be large and nonlinearly related to the volt-seconds seen on the secondary. With forwards, constant frequency operation is most typical. With flybacks, it is possible to make high performance variable frequency units by triggering the turn on of a given cycle on the resetting of the transformer from the previous cycle. This causes the converter to operate at the boundary separating continuous and discontinuous modes, with the ease of compensation of the former and the simplicity and low-switching losses of the latter.

The overall control scheme, as shown in Figure 13, including the error amplifier and turn-off circuitry on the secondary with a simple pulse feedback, is described in US patent 4,323,961. This patent, along with a number of related patents, are assigned to Astec and are not in the public domain. License will be granted for the use of these patented techniques and circuits when applying the AS4301. Any other use of these circuits may be in violation of applicable patent laws.

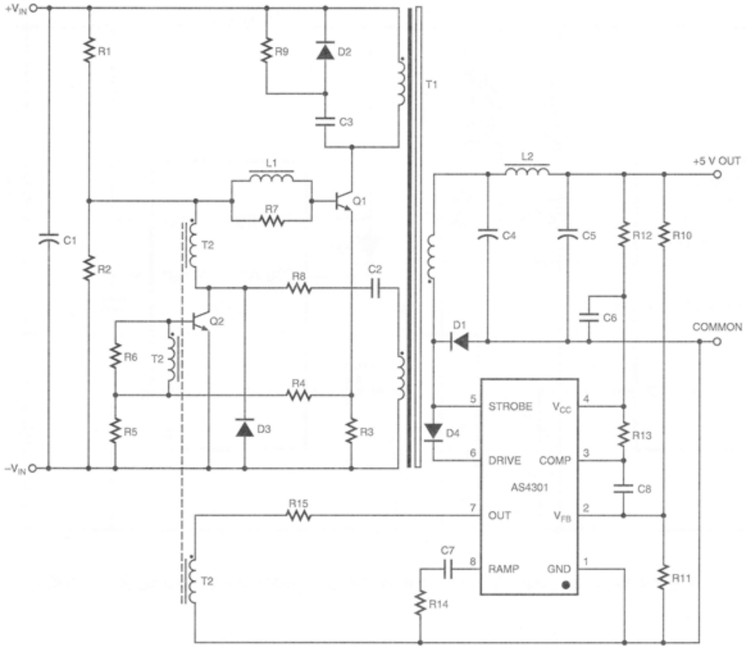


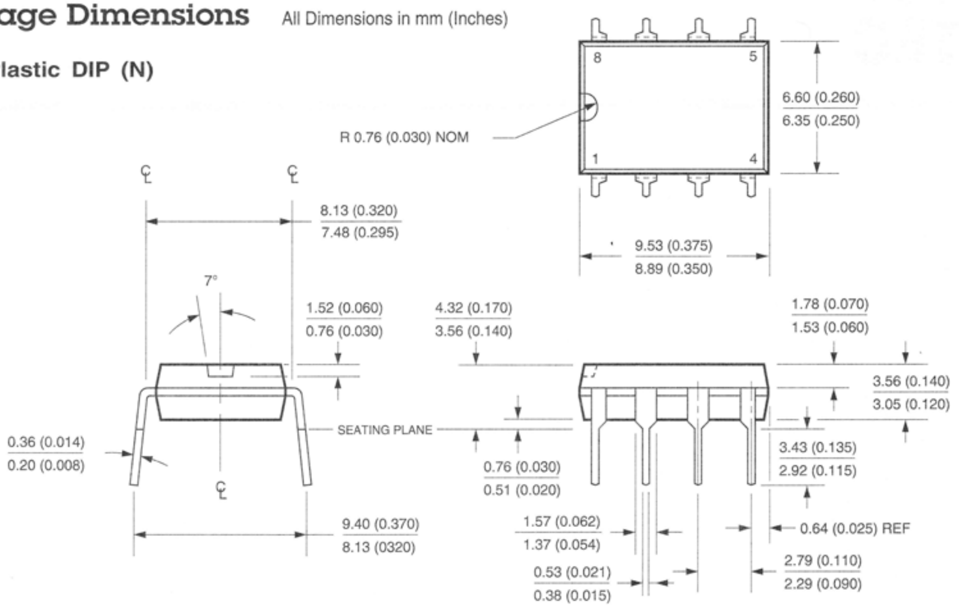
Figure 13. Simplified Isolated Flyback Converter

This circuit is simplified in order to illustrate the general control scheme made possible by the AS4301. This flyback topology is protected by U.S. Patent #4,323,961 and it's description implies no license for use. The AS4301 Secondary Controller IC has been specifically designed to implement the ASTEC patented Flyback Conversion Circuit. Inclusion of the AS4301 in a power supply will license that product for the Flyback topology protected by the U.S. Patent #4,323,961.

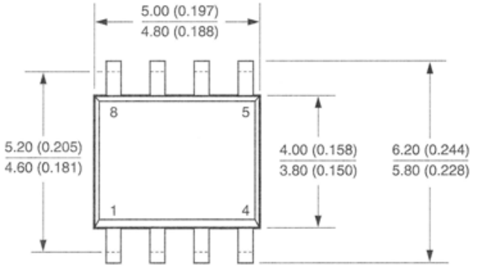
Package Dimensions

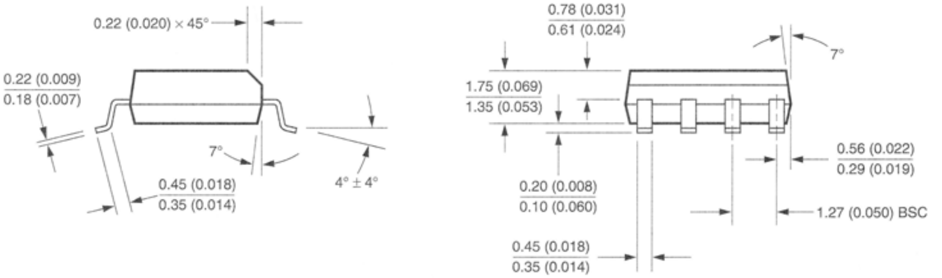
All Dimensions in mm (Inches)

8-Pin Plastic DIP (N)



8-Pin Plastic SOIC (D)





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Notes

ASTEC

AS273

Over-Temperature Detector

Features

- Programmable to three different Over-temperature thresholds
- 2.5 V temperature compensated bandgap reference trimmed to 1%
- Open collector output goes low on over-temp condition
- ±3° C temperature accuracy
- Reference shunt current serves to program over-temp threshold
- Available with 5° C or 10° C of temperature hysteresis
- Available in a wide range of over-temp thresholds to fit most temperature monitoring applications
- Now available in the SOT-223 for improved substrate temperature sensing

Description

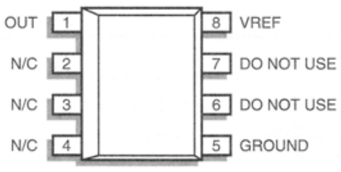
The AS273 is a series of programmable over-temperature detectors. Each is internally composed of a precision 2.5 V shunt reference, a proportional-to-absolute temperature thermal sensor, a comparator with controlled hysteresis, and an open collector output that indicates an over-temp condition. The threshold for the over-temp signal can be set to any of three values on a given part by controlling the magnitude of the reference shunt current.

The AS273 has an excellent absolute temperature accuracy of ±3° C for each of the three over-temp thresholds. The low power dissipation minimizes any temperature sensing errors due to self-heating. There is either 5° C or 10° C of temperature hysteresis to prevent bouncing when an over-temp condition is removed.

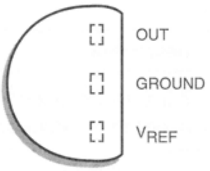
The packaging options available with the AS273 make it appealing to a wide variety of temperature-sensing applications. The TO-237 package with a built-in heat sink allows for highly accurate ambient temperature sensing. The TO-92 package can be mechanically clamped to a heat sink to monitor the temperature of power devices. The 8L-SOIC and SOT-223 surface mount packages allow for temperature sensing in high component density applications.

Pin Configuration — Top view

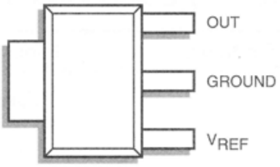
SOIC (D)



TO-92 (LP), TO-237 (HP)



SOT-223 (G)



Ordering Information

AS273 - T H - P

Temperature Option see A

Hysteresis Option see C

Package Type see B

A. Temperature Options

Code	T_{OT1}	T_{OT2}	T_{OT3}
D	40	45	50
F	75	80	85
G	90	95	100
H	105	110	115

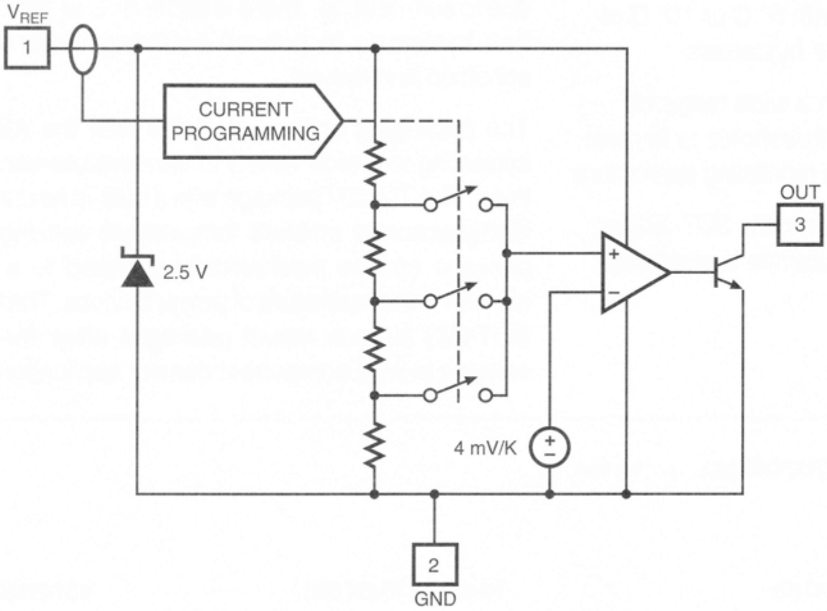
B. Package Types

Code	Package
HP	TO-237
LP	TO-92
D	SOIC-8
G	SOT-223

C. Hysteresis Options

Code	Temp. Hysteresis
1	10° C
5	5° C

Functional Block Diagram



Pin Function Description

Pin Number	Function	Description
1	V_{REF}	2.5 V shunt reference; current into V_{REF} pin also programs over-temperature trip point to one of three T_{OT} values
2	GND	Circuit ground and silicon substrate
3	OUT	Open collector output. Output low when die temperature exceeds programmed trip point

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Reference Current	V_{REF}	±10	mA
Output Current	I_{OUT}	±10	mA
Output Voltage	V_{OUT}	18	V
Continuous Power Dissipation at 25° C			
TO-92	P_D	775	mW
TO-237	P_D	1000	mW
8-SOIC	P_D	750	mW
SOT-223	P_D	1000	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−65 to 150	°C
Lead Temp, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
SOT-223	115° C/W	8° C/W	8.7 mW/°C
TO-92	160° C/W	80° C/W	6.3 mW/°C
TO-237	125° C/W	8° C/W	8.0 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C

Electrical Characteristics

Electrical Characteristics are guaranteed over the full junction temperature range (0 to 125° C). Ambient temperature must be derated based upon power dissipation and package thermal characteristics.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference						
Reference Voltage	V_{REF}	$I_{REF} = 2$ mA, $T_J = 25°$ C	2.500	2.525	2.550	V
Load Regulation	V_{ld}	0.65 mA $\leq I_{REF} \leq 5.5$ mA		5	10	mV
Average Temperature Coefficient	$\Delta V_{REG}/\Delta T$	0.65 mA $\leq I_{REF} \leq 5.5$ mA		75		ppm/°C
Output						
Saturation Voltage	V_{OL}	$I_{OUT} = 4$ mA; $T_J > T_{OT}$		200	400	mV
Breakdown Voltage	BV	$I_{OUT} = 4$ µA; $T_J < T_{OT}$	18	30		V
Leakage Current	I_{OH}	$V_{OUT} = 18$ V; $T_J < T_{OT}$		1	1000	nA
Over-Temp Sensing						
Temperature Accuracy	$T_{OT(1)}$	0.7 mA $\leq I_{REF} \leq 1.3$ mA	−3		+3	°C
	$T_{OT(2)}$	1.55 mA $\leq I_{REF} \leq 2.6$ mA	−3		+3	°C
	$T_{OT(3)}$	3.0 mA $\leq I_{REF} \leq 5.0$ mA	−3		+3	°C
Hysteresis	H_{OT}	Percentage Error in Nominal Hysteresis	−30		+30	%

Test Circuit

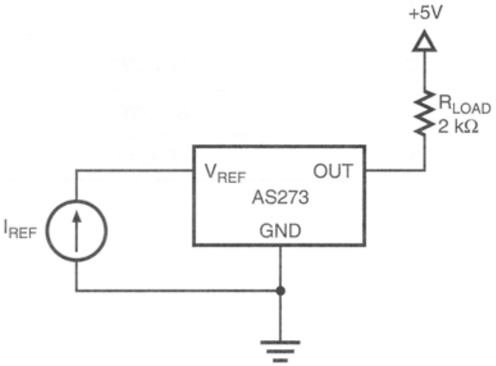


Figure 1. Test Circuit for Output Hysteresis Curve

Typical Performance Curves

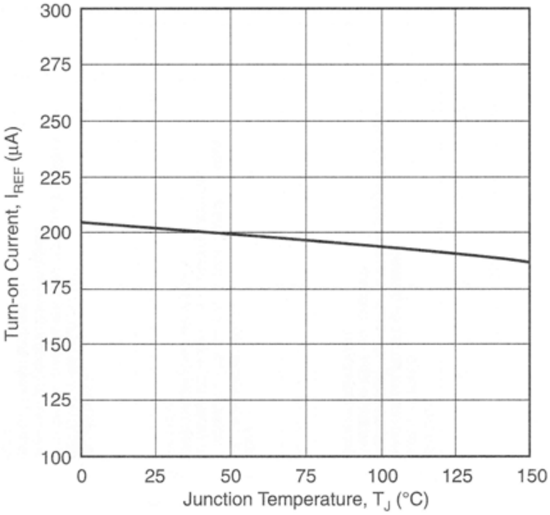

Minimum Reference Current for Regulation

Figure 2

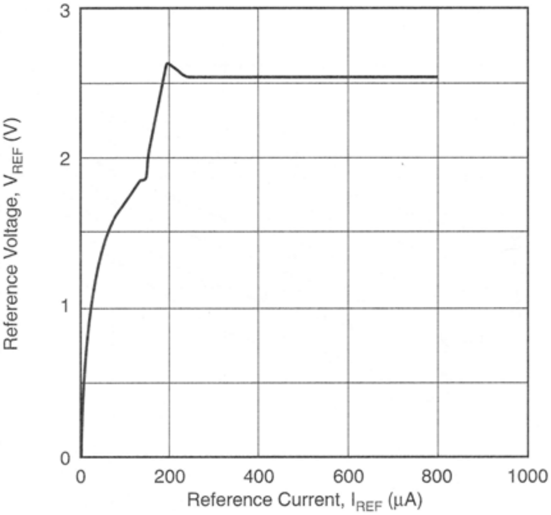

Turn-on Characteristic of Reference

Figure 3

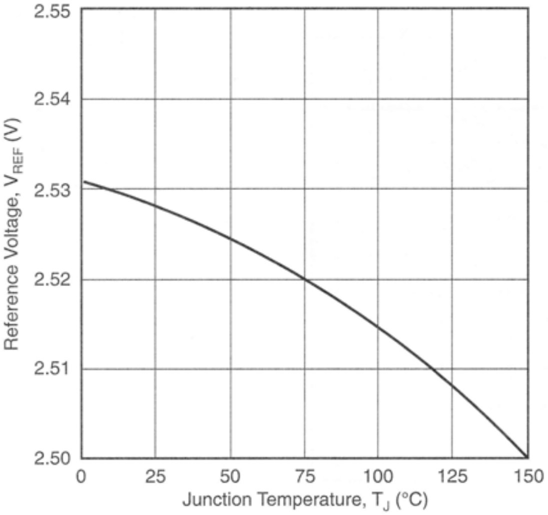

Temperature Regulation of Reference

Figure 4

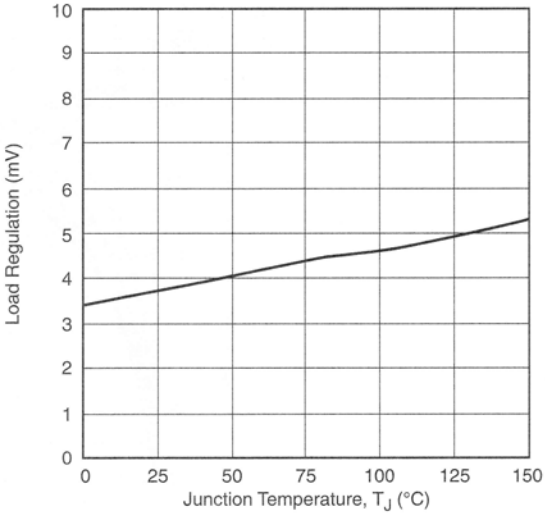

Load Regulation of Reference Over-temperature

Figure 5

Typical Performance Curves

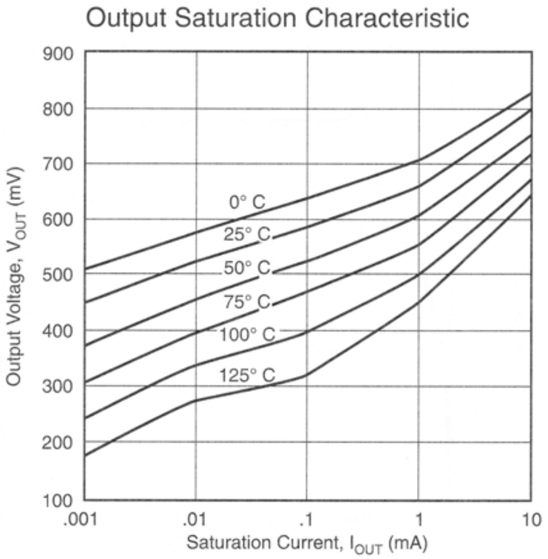


Figure 6

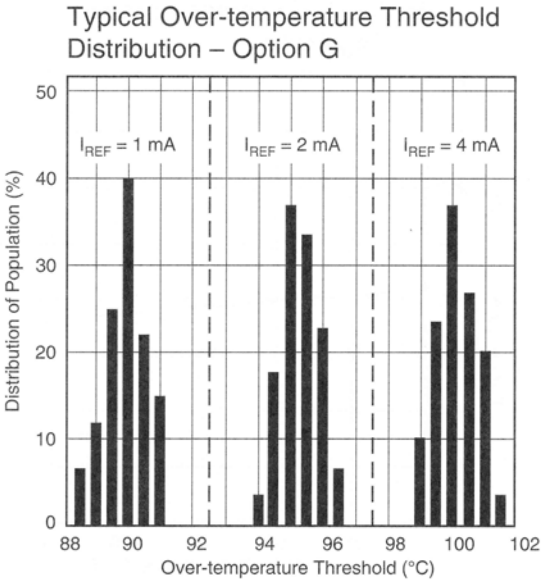


Figure 7

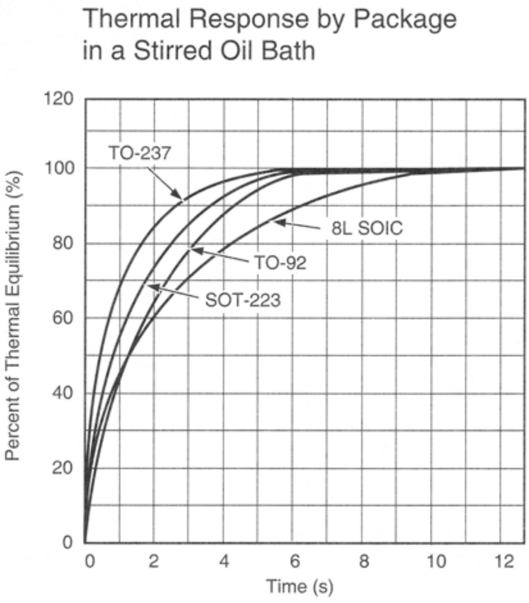


Figure 8

Theory of Operation

The AS273 is an over-temperature detector that gives an over-temp signal when the device juction temperature exceeds a programmed over-temp threshold. Over-temp threshold programming is accomplished by controlling the magnitude of the reference shunt current.

Overtemperature Condition

Internal to the AS273 is a temperature sensor which creates a voltage proportional to the absolute temperature(PTAT) of the die. This PTAT voltage is compared with a fraction of the reference voltage corresponding to the over-temperature threshold. When the PTAT voltage exceeds the reference voltage, the comparator is tripped and an over-temp signal is given to the output. The output consists of an open collector transistor that pulls low on an over-temp condition. Built into the comparator is temperature hysteresis, which keeps the over-temp signal until the junction temperature has fallen 5° C (or 10° C) below the over-temp threshold. Figure 9 shows the output of the AS273 (with 10° C of hysteresis) over a range of junction temperature.

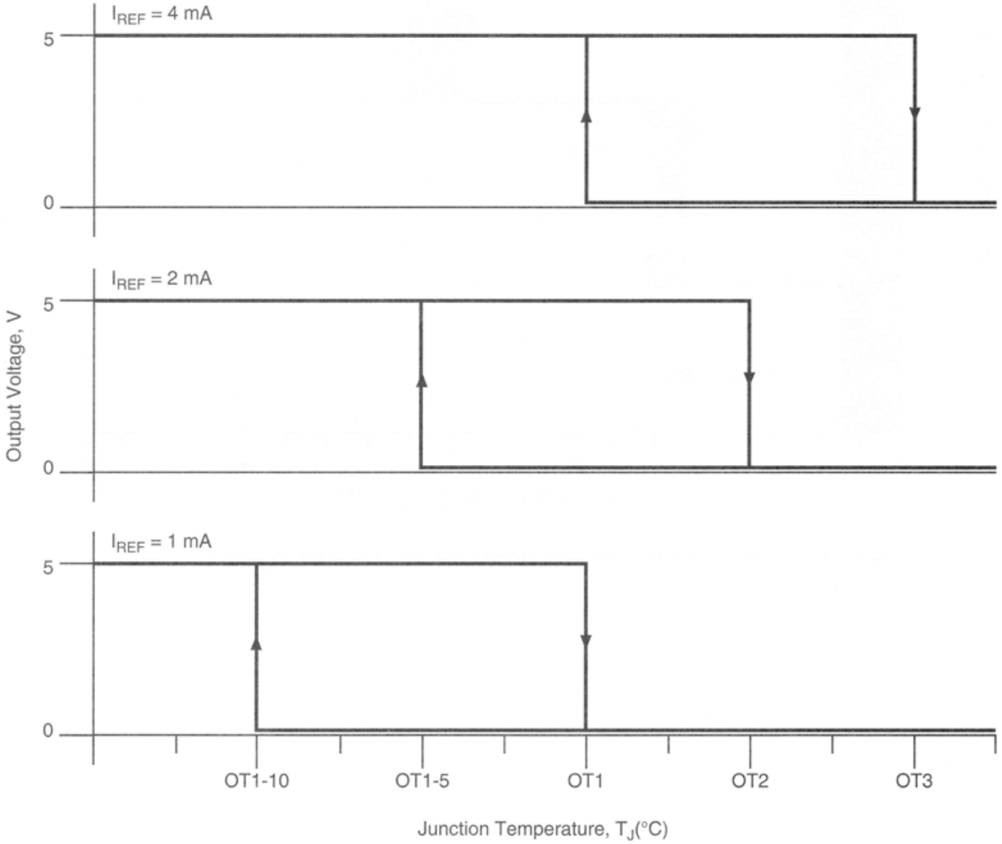


Figure 9. Temperature Characteristic of Output with 10° C of Hysteresis

Current Programming

There are three different over-temp thresholds for each AS273. The detector senses the amount of current being shunted through the 2.5 V reference of pin 1 and programs an over-temp threshold based on the magnitude of that current. Figure 10 illustrates the ranges of reference shunt current, I_{REF}, associated with each of the three over-temp thresholds, OT1, OT2 and OT3.

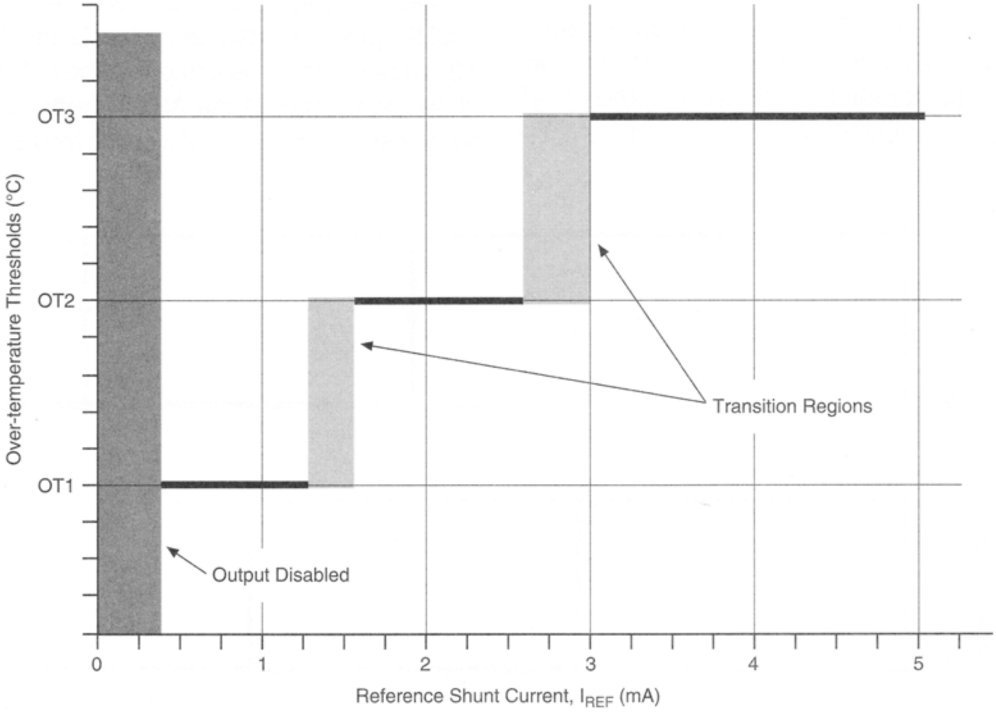


Figure 10. Reference Shunt Current Programming Ranges of Over-temperature Thresholds

Typical Over-Temperature Detector Applications

Over-Temperature Detector

The AS273 senses the ambient temperature and turns on its open collector output to indicate an over-temp condition. Each AS273 can be programmed to any one of its three over-temp thresholds by forcing a different range of current into the reference pin.

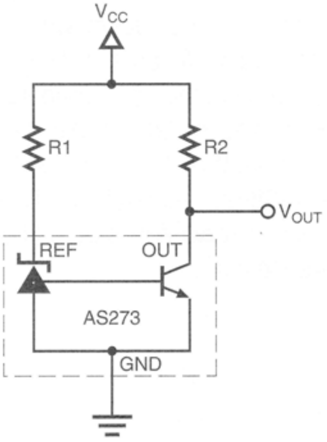


Figure 11.

Dual Speed Fan Control

The diagram of Figure 12 shows an easy way to implement smart fan control. When the temperature is below the over-temp trip point set by R1, the detector's open collector output is off. Therefore, the fan speed is controlled by the ratio between R2 and R3. When the temperature exceeds the over temp set point, the open collector is turned on, and fan motor runs at its full speed.

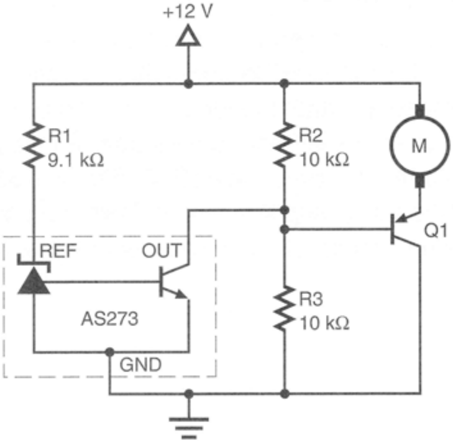


Figure 12.

Over-Temperature Protection with Latch (Low Current)

The diagram of Figure 13 illustrates how a power supply can be shut down with a simple two-transistor latch. When the programmed over-temp is reached, the open collector output of the AS273 enables the latch and pulls V_{CC} below the under-voltage threshold of the AS3842 ,shutting off the AS3842. The latch can be disabled only with a power reset.Adjustable Hysteresis Temperature Detector

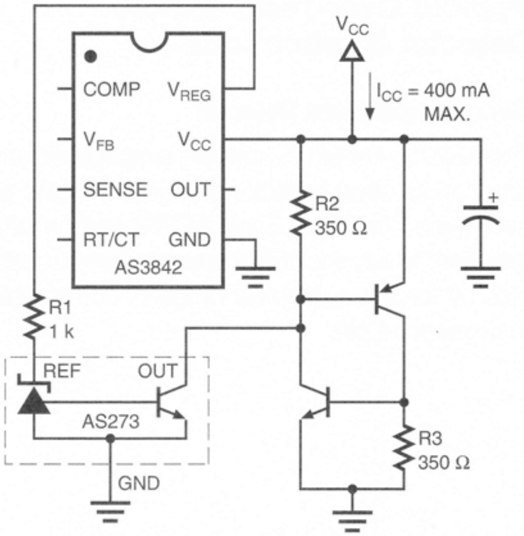


Figure 13.

Over-Temperature Protection with Hysteresis

In this over-temperature circuit, the hysteresis of the AS273 is used to automatically restart the power supply after the temperature drops below the hysteresis temperature window. R1 supplies the current to power the AS273 after the AS3842 and the power supply are shut down. R2 and the external zener set the over temperature trip point.

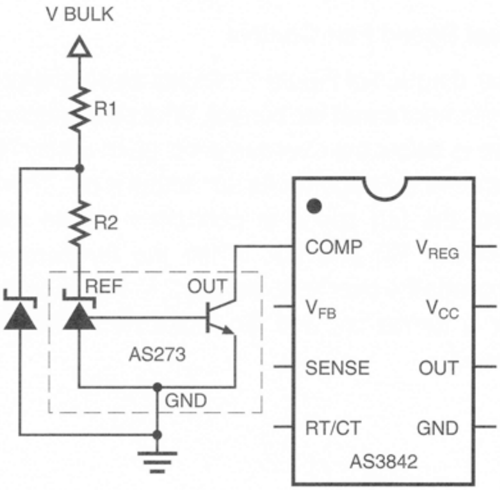


Figure 14.

Adjustable Hysteresis Temperature Detector

The hysteresis of the AS273 can be increased by reprogramming the device to a lower temperature set point upon over-temp. A higher temperature is set by R1. When the temperature exceeds the high-temp set point, the open collector output is turned on and allows R2 to rob current from the reference pin and resets the AS273 to the low-temp set point. As a result, the hysteresis escalates by the difference between the high-temp and the low-temp set points.

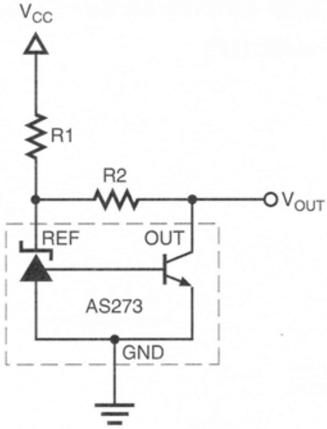
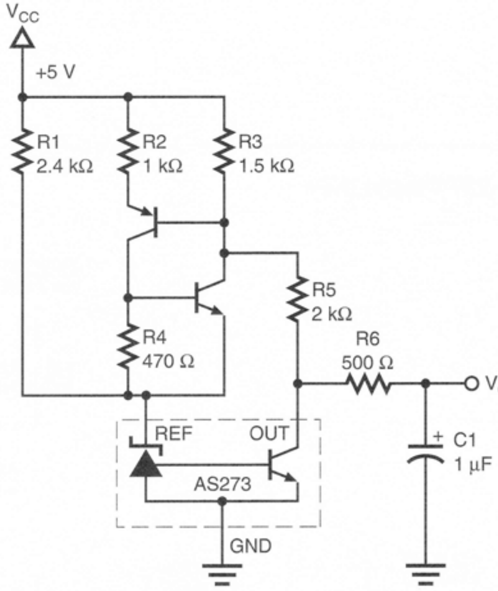


Figure 15.

Three-State Temperature Sensor

In the Three-State Temperature Sensor shown in Figure 16, a low-temp trip point is selected by R1 and a high-temp trip point is selected by the two-transistor latch. When the temperature is below the low-temp set point, V_{OUT} is in the high state (V_{OUT} = 5.0 V). When the temperature exceeds the low-temp set point, the two-transistor latch is set and V_{OUT} is pulled low (V_{OUT} = 2.5 V). The latch also supplies extra current to the reference pin to reset the IC to sense a higher temperature. Once the high-temp is reached, the output will turn "on" (V_{OUT} = 0.2 V). This circuit is highly useful in applications where a stand-by, a warning and a shut-down state are required.



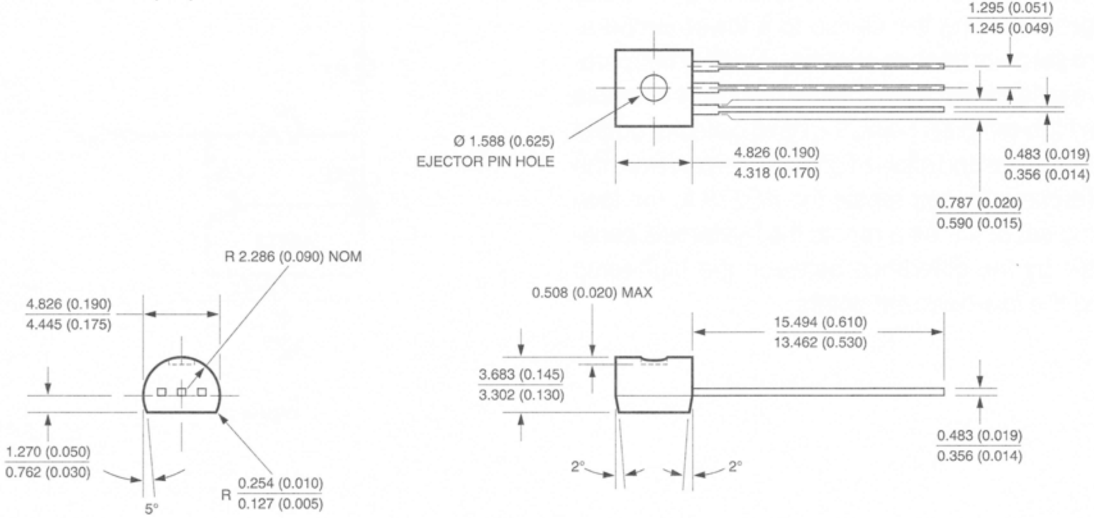
Stand-by State:	T < T1, T2	V_O = 5.0 V
Warning State:	T1 < T < T2	V_O = 2.5 V
Shut-down State:	T1, T2 < T	V_O = 0.2 V

Figure 16.

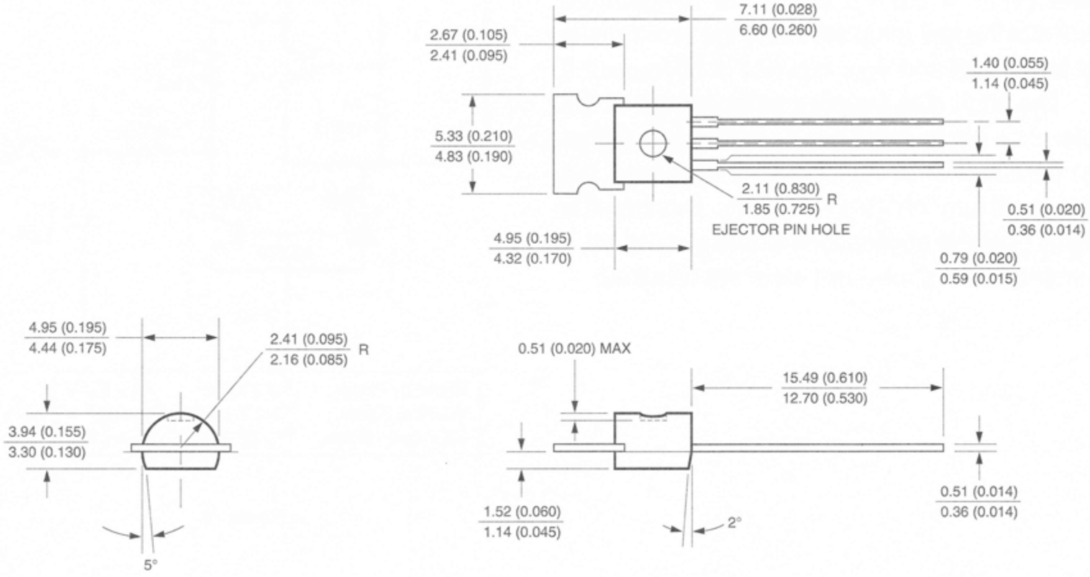
Package Dimensions

All Dimensions in mm (Inches)

TO-92 Plastic (LP)



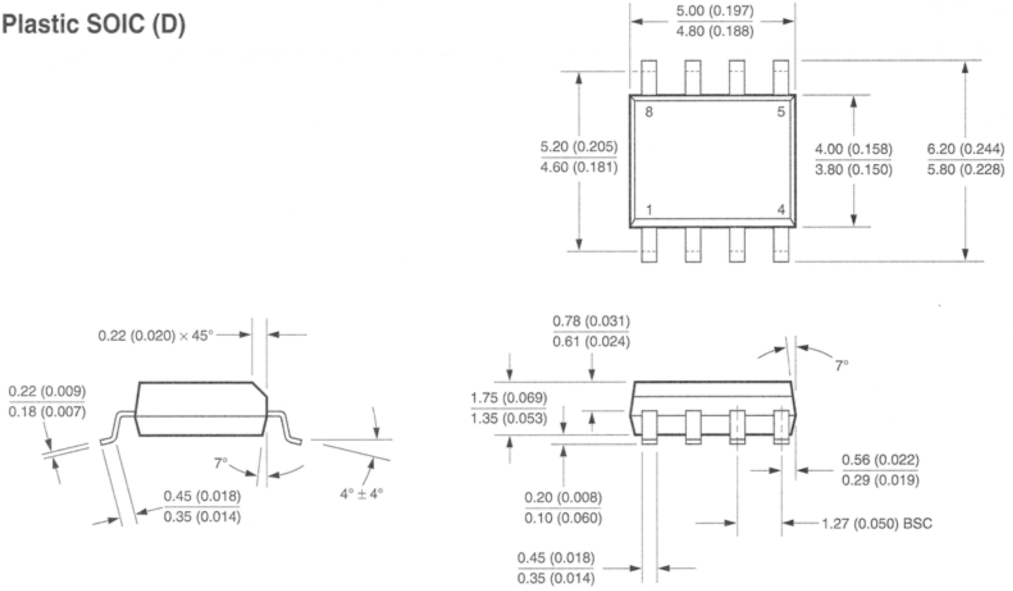
TO-237 Plastic (HP)



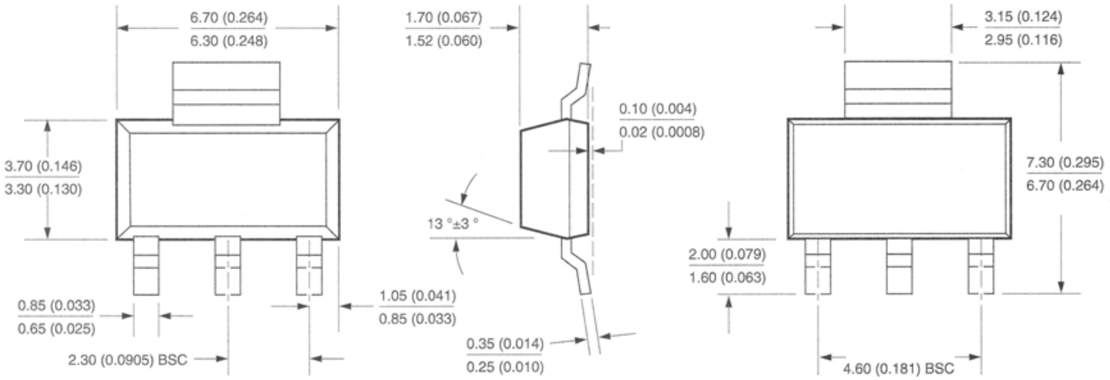
Package Dimensions

All Dimensions in mm (Inches)

8-Pin Plastic SOIC (D)



SOT-223(G)



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Notes

ASTEC

AS1200

Power Good Circuit

Features

Under-Voltage Sense

- Senses:

  2 Positive supplies

  2 Negative supplies

  AC mains

- Programmable delay open collector output

Over-Voltage Sense

- Senses:

  1 Positive supply

  1 Negative supply

- Robust follower output

Reference

- Low TC Bandgap
- Trimmed for accuracy
- Output impedance ≤ 2 Ω

Description

The AS1200 Power Good Circuit is a general purpose housekeeping circuit for multiple output power supplies. The AS1200 is comprised of a precision bandgap reference, under-voltage detection circuitry and over-voltage detection circuitry.

Upon detection of under-voltage or power failure, the Power OK output immediately turns on (active low). Once tripped, the POK signal returns high again only after a programmable delay to ensure the power supply resumed normal operation.

The over-voltage circuit provides an active high signal whenever over-voltage is detected in either a positive or negative supply. The OVP output is a high current emitter follower, suitable for driving either an opto-isolator or an SCR crowbar.

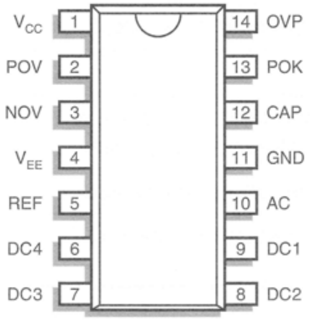
Both the under-voltage and over-voltage circuits use single-ended comparators that are internally referenced to a 2.5 V shunt reference. Although designed to be operated under a narrow range of shunt currents, this bandgap reference is extremely stable, temperature compensated and trimmed to give a tight production tolerance.

Ordering Information

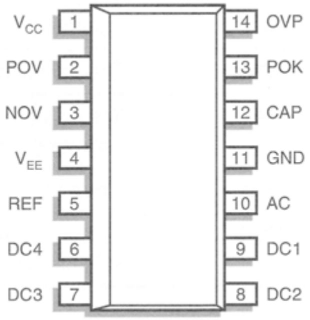
Description	Temperature Range	Order Code
14-Pin Plastic DIP	0 to 70° C	AS1200N
14-Pin Plastic SOIC	0 to 70° C	AS1200D

Pin Configuration — Top view

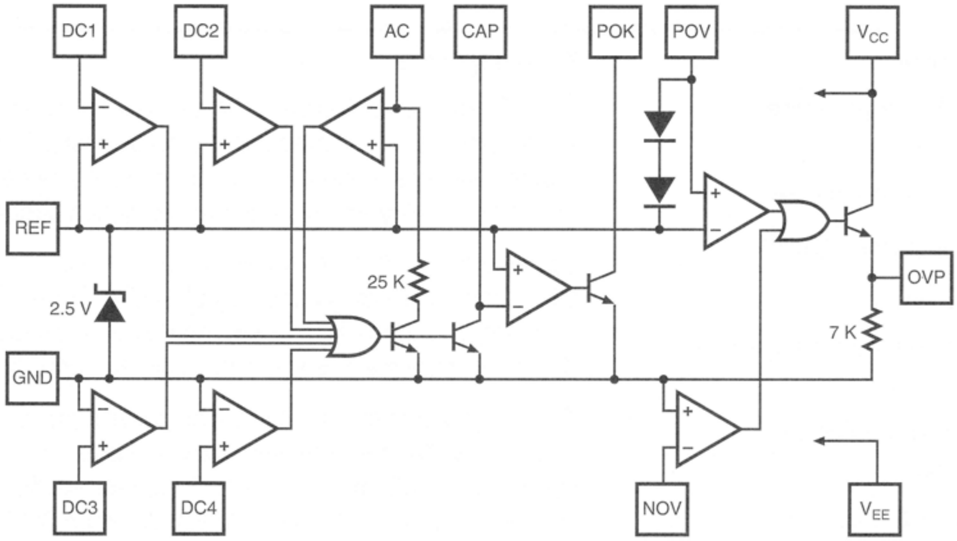
PDIP (N)



SOIC (D)



Functional Block Diagram



Pin Function Description

Pin Number	Function	Description
1	V_{CC}	Positive power input to the chip.
2	POV	Input for sensing over-voltage of positive rails.
3	NOV	Input for sensing over-voltage of negative rails.
4	V_{EE}	Negative power input to the chip.
5	REF	Shunt voltage reference, nominal 2.5 V.
6	DC4	Input for sensing under-voltage of a negative rail.
7	DC3	Input for sensing under-voltage of a negative rail.
8	DC2	Input for sensing under-voltage of a positive rail.
9	DC1	Input for sensing under-voltage of a positive rail.
10	AC	Input for sensing low voltage or shutdown of AC supply.
11	GND	Ground connection for the chip.
12	CAP	Timing input for providing the delay between all the rails becoming good and allowing the POK signal to go high.
13	POK	Open collector output of the under-voltage comparators.
14	OVP	Emitter follower output of the over-voltage comparators, suitable for driving crowbars.

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Continuous Power Dissipation at 25° C	P_D		
14L SOIC		950	mW
14L PDIP		1400	mW
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	12	V
	V_{EE}	−12	V

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
14L SOIC	130° C/W	35° C/W	7.7 mW/°C
14L PDIP	120° C/W	28° C/W	8.3 mW/°C

Electrical Characteristics

Unless otherwise stated, all parameters tested over the following range of conditions:
V_{CC} = 5 V to 18 V; V_{EE} = −2 V to −14 V; T = 25° C; I_{REF} = 4 mA to 8 mA

Parameter		Condition	Min	Typ	Max	Units
Reference						
Reference Voltage		(Over Full Line, Load, and Temp)	2.45	2.49	2.55	V
Output Resistance		I_{REF} From 4 mA to 8 mA		1	12	Ω
Temperature Deviation		0 to 70° C		6	17	mV
Supply Rejection		+5/−2 V to + 18/−14 V		2	15	mV
Under-voltage (Supplies +5/−2 V to ±14 V)						
DC1, DC2 Sense Voltage			2.43	2.46	2.53	V
Input Current	(high)	DC1, DC2 = 3 V	0	1	4	µA
Input Current	(low)	DC1, DC2 = 2 V	−0.2	0	0.2	µA
DC3, DC4 Sense Voltage		(From REF)	2.43	2.49	2.53	V
Input Current	(high)	DC3, DC4 = 1 V	0	1	4	µA
Input Current	(low)	DC3, DC4 = −1 V	−0.2	0	0 .2	µA
Offset Voltage:	DC3 DC4		−10 −20	10 10	30 40	mV mV
AC Sense Voltage			2.43	2.46	2.53	V
Input Current	(high)	AC = 3 V	0	1	4	µA
Input Current	(low)	AC = 2 V	50	80	120	µA

Electrical Characteristics (cont'd)

Unless otherwise stated, all parameters tested over the following range of conditions:
V_{CC} = 5 V to 18 V; V_{EE} = –2 V to –14 V; T = 25° C; I_{REF} = 4 mA to 8 mA

Power OK Circuit					
CAP:					
I_{OH} (no under-voltage)	CAP = 3 V	–10	0	100	nA
I_{OH} (charging CAP)	CAP = 2 V	–1	–0.02	0.01	µA
I_{OL} (under-voltage)	CAP = 3V	0.2	10		mA
V_{OL} (under-voltage)	I_{CAP} = 100 µA	0	35	100	mV
CAP Sense Voltage		2.40	2.49	2.55	V
POK:					
I_{OH} (no under-voltage)	POK = 5 V			1	µA
I_{OL} (under-voltage)	POK = 0.4 V	20	50		mA
V_{OL} (under-voltage)	I_{POK} = 10 mA		60	200	mV
Over-Voltage					
POV Sense Voltage		2.41	2.46	2.52	V
Input Current	POV = 3 V		1	4	µA
NOV Sense Voltage		0		100	mV
Input Current	NOV = 1 V		1	4	µA
OVP OUTPUT:					
V_{OH} (over-voltage)	V_{CC} = 18 V, I_{OVP} = 0 mA	15.5	16.5		V
	I_{OVP} = 100 mA	15.0	15.2		V
	V_{CC} = 5 V, I_{OVP} = 0 mA	2.5	3.5		V
	I_{OVP} = 100 mA	2.2	3.2		V
I_{OH} (over-voltage)	V_{CC} = 12 V, OVP = 1.4 V		500		mA
V_{OL} (no over-voltage)			0.5	100	mV
Power					
I_{CC} (fault: OVP, POK on)	V_{CC} = 18 V		7	16.5	mA
	V_{CC} = 5 V		3.5	6	mA
I_{EE}	V_{EE} = –14 V		3.5	5	mA
	V_{EE} = –2 V		3	4.5	mA

Typical Performance Curves

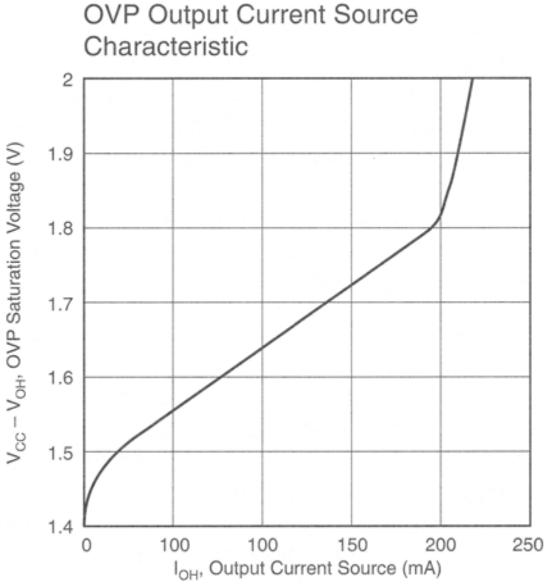


Figure 1

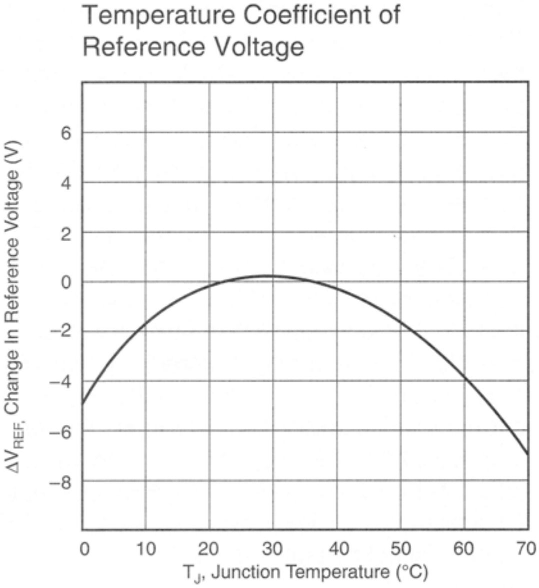


Figure 2

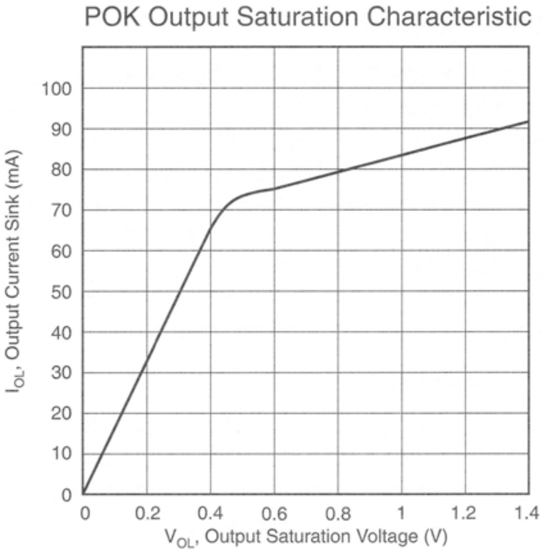


Figure 3

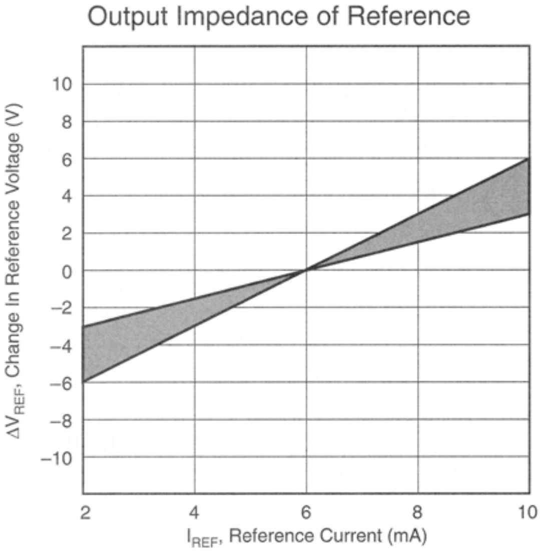


Figure 4

Theory of Operation

Over-Voltage Sense

The over-voltage sense circuitry consists of the Positive Over-Voltage (POV) Sense comparator, the Negative Over-Voltage (NOV) Sense comparator and the Over-Voltage Protection (OVP) output. The POV comparator (Pin 2) is internally referenced to the 2.5 V_{REF} (Pin 5) and the NOV comparator is referenced to the Ground line (Pin 11). Both these comparators have NPN inputs. The NOV input is unprotected and must not be pulled more than 5 V from Ground. The POV input is the only protected NPN input on the AS1200. It is internally clamped by two diode drops to the 2.5 V reference. Thus, any excess current used in driving the POV input high will be dumped into the REF bus and will contribute to the effective REF bias current. (See REF description for limitations on REF bias current.) The POV input must not be pulled more than 5 V below the REF voltage.

The OVP output (Pin 14) is an NPN Darlington follower which actively pulls to within 2 V of V_{CC}. It is an active high output, so when an over-voltage condition is detected by either POV or NOV, OVP goes high and is capable of sourcing 500 mA typically, sufficient for the gate drive of an SCR crowbar or for an opto-isolator type load. When no over-voltage condition exists, the OVP output is low and is internally pulled to Ground by a 7kΩ resistor.

Under-Voltage Detection

The under-voltage detection circuit consists of the DC rail under-voltage sense comparators DC1, DC2, DC3 and DC4, the AC under-voltage sense comparator AC, the external timing RC pin CAP, and the power OK output POK. All the comparators have unprotected NPN inputs and must not be pulled more than 5 V from their nominal trip points, as with the NOV input described above. DC1 (Pin 9), DC2 (Pin 8) and AC (Pin 10) are referenced to the 2.5 V_{REF}, and DC3 (Pin 7) and DC4 (Pin 6) are referenced to the Ground line. All comparator inputs will clamp to V_{CC} when pulled high.

DC1 and DC2 are used to detect under-voltage in the outputs of positive supplies. DC3 and DC4 are used to detect under-voltage in the outputs of negative supplies, and the AC comparator is used to detect power failure in the AC mains. The AC comparator is essentially identical to the positive DC comparators except for a 25 k resistor which creates hysteresis by pulling down on the AC input whenever under-voltage has been detected.

The CAP pin (Pin 12) is the open collector output of the logical OR of the under-voltage sense comparators, and it can sink several milliamps. It is also the high impedance input to the power OK comparator. Thus, an external RC can be applied to this pin which will discharge quickly under a fault (under-voltage) condition, yet return to a high state (power OK) condition slowly, the timing set by the external RC. The power OK comparator's nominal trip point is the 2.5 V_{REF}. The CAP pin will clamp to V_{EE}. The output of the power OK comparator is POK (Pin 13). This is a TTL compatible open collector output which clamps at V_{EE}.

Shunt Reference

The REF pin (Pin 5) is a shunt reference with nominal value of 2.5 V. As a shunt design, it must sink current to operate (*i.e.*, via an external pullup). It is an extremely stable bandgap which is trimmed for a tight production tolerance. However, it is designed to operate over a narrow range of shunt currents, 4 to 8 mA. To obtain the specified output impedance, care must taken to operate the reference within the specified range of shunt currents.

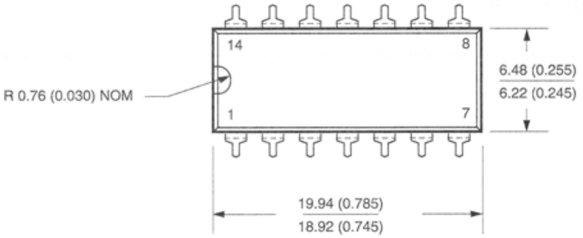
Chip Biasing

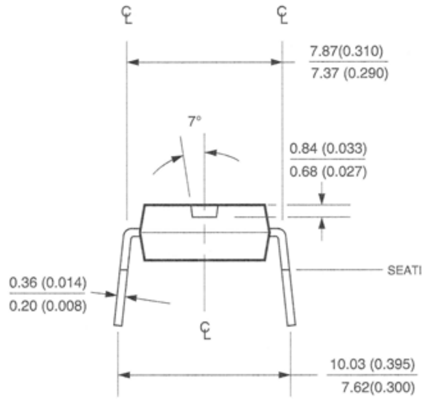
V_{CC} (Pin 1) may operate in the range of 5 to 18 V (12 V nominal). Ground (Pin 11) is the signal common to the comparators and the shunt reference. V_{EE} (Pin 4) is the substrate connection which must be pulled a minimum of 2 and a maximum of 14 V negative with respect to the Ground line.

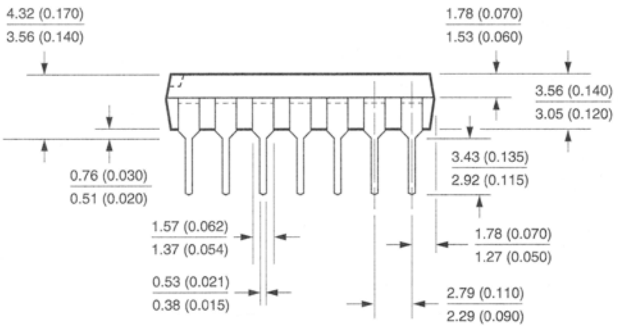
Package Dimensions

All Dimensions in mm (Inches)

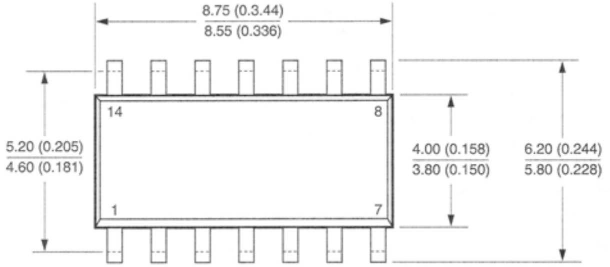
14-Pin Plastic DIP (N)

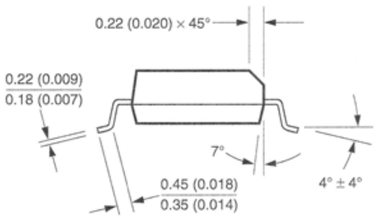


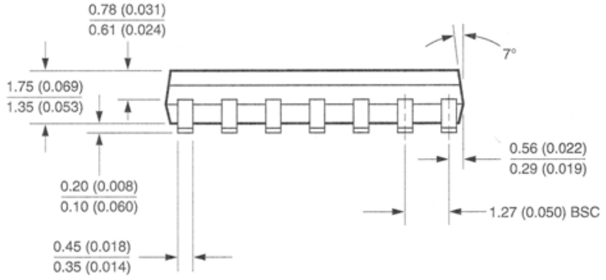




14-Pin Plastic SOIC (D)







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ASTEC SEMICONDUCTOR

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Notes

ASTEC

AS23xx

Secondary Side Housekeeping Circuit

Proposed Specification

Description

The AS23xx is a family of housekeeping circuits for monitoring the outputs of power supplies. They directly sense all the output rails without the need for external dividers and detect undervoltage and overvoltage. They also provide an additional undervoltage comparator which may be configured with any arbitrary hysteresis to sense a divided down representation of the AC bulk voltage. The housekeeping section provides all the features necessary to allow external caps to set the common timing features of PC type power supplies. In addition, negative rails may be sensed without the necessity of a V_{EE} connection, and negative sensing may be disabled without affecting operation of the positive sense section. An error amplifier is also available for use in output sensing and feedback to the control circuitry. As an option, it may be internally referenced to 3.3 V. The 3.3 V series reference is available and can source up to 5 mA.

This IC will be available in a variety of pin configurations in 14, 16 and 18 lead packages. See the pin description table on page 3 for the features available.

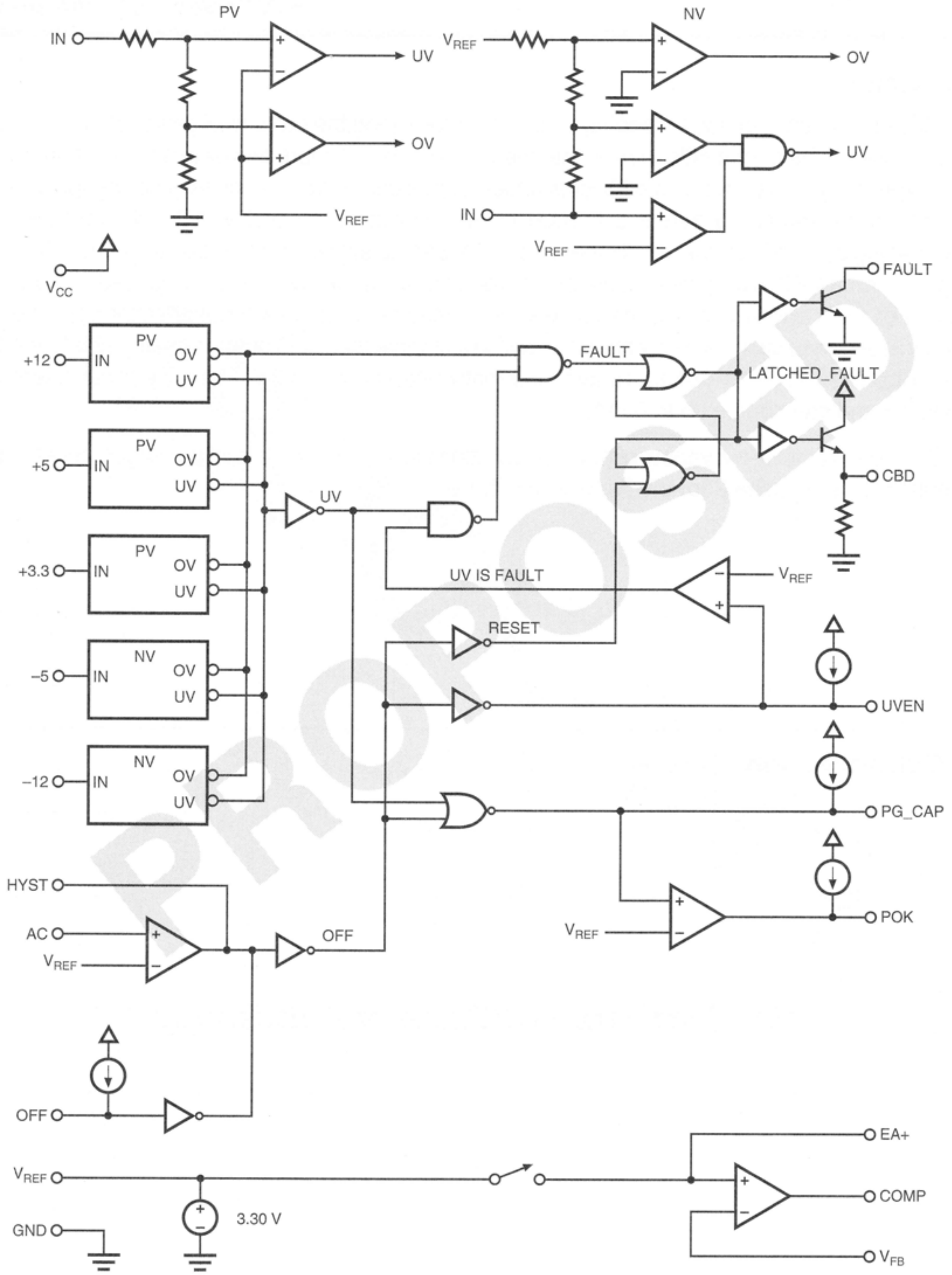
PROPOSED

Pin Configuration — Top view

Not Available at Time of Publishing

Functional Block Diagram

PROPOSED



Pin Function Description

PROPOSED

Pin Number	Function	Description
1	+3.3 V	Input for overvoltage and undervoltage for the +3.3 V rail.
2	+5 V	Input for overvoltage and undervoltage for the +5 V rail.
3	+12 V	Input for overvoltage and undervoltage for the +12 V rail.
4	–5 V	Input for overvoltage and undervoltage for the –5 V rail. This function may disabled by tying this pin to a positive voltage above 3.5 V.
5	–12 V	Input for overvoltage and undervoltage for the –12 V rail. This function may disabled by tying this pin to a positive voltage above 3.5 V.
6	PG CAP	A cap to ground provides a delay between undervoltage sensing becoming good and the POK output going high.
7	UVEN	This pin may be grounded to prevent undervoltage conditions from triggering the FAULT signal. A cap to ground provides start-up blanking of the undervoltage sensing portion of the FAULT signal.
8	AC	Non-inverting input to the AC undervoltage sensing comparator.
9	HYST	Open collector output of the AC undervoltage comparator. A resistor between this pin and AC will provide hysteresis to the AC undervoltage sensing.
10	POK	Open collector output of the undervoltage sensing comparators. This pin goes low upon an undervoltage condition. Except for the delay set by the PG CAP, this pin always reflects the actual state of the undervoltage sensing.
11	FAULT	Open collector output of the overvoltage and undervoltage comparators.
12	CBD	Optional crow bar drive output of the FAULT function.
13	EA+	Non-inverting input to the error amplifier.
14	V_{FB}	Inverting input to the error amplifier.
15	COMP	Output of the error amplifier.
16	OFF	Pulling this pin low will reset the FAULT latch and discharge the start-up timing capacitors, START CAP and PG CAP.
17	V_{REF}	3.3 V Voltage reference. This is a series regulator type reference.
18	GND	Signal ground and silicon substrate.
19	V_{CC}	Power input to the chip.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	20	V
Continuous Power Dissipation at 25° C	P_D	N/A	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PROPOSED

Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are V_{CC} = 12 V; +3.3 V = 3.3 V; +5 V = 5V; +12 V = 12 V; −12 V = −12 V; −5 V = −5 V.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Bias						
Supply Current	I_{CC}			8	10	mA
Undervoltage, Overvoltage **+3.3 V**						
+3.3 V Undervoltage	UV		2.98	3.06	3.14	V
+3.3 V Overvoltage	OV		3.77	3.96	4.16	V
+3.3 V Input Current	I_B			0.5	1	mA
+5 V						
+5 V Undervoltage	UV		4.50	4.63	4.75	V
+5 V Overvoltage	OV		5.70	6.00	6.30	V
+5 V Input Current	I_B			0.5	1	mA
+12 V						
+12 V Undervoltage	UV		10.5	10.8	11.0	V
+12 V Overvoltage	OV		13.5	14.3	15.0	V
+12 V Input Current	I_B			0.5	1	mA
−5 V						
−5 V Undervoltage	UV		−4.30	−4.40	−4.50	V
−5 V Overvoltage	OV		−5.70	−6.00	−6.30	V
−5 V Input Current	I_B			−0.5	−1	mA
−5 V Disable Voltage	V_D	Minimum voltage to disable		3.3	4.0	V

Electrical Characteristics (cont'd)

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are V_{CC} = 12 V; +3.3 V = 3.3 V; +5 V = 5V; +12 V = 12 V; –12 V = –12 V; –5 V = –5 V.

PROPOSED

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
–12 V						
–12 V Undervoltage	UV		–10.2	–10.5	–10.8	V
–12 V Overvoltage	OV		–13.5	–14.3	–15.0	V
–12 V Input Current	I_B			–0.5	–1	mA
–12 V Disable Voltage	V_D	Minimum voltage to disable		3.3	4.0	V
AC/HYST						
AC Undervoltage	UV		3.25	3.30	3.35	V
AC Input Current	I_B			–0.5	–1	µA
HYST High State Leakage	I_L	V_O = 5 V		0.01	1	µA
HYST Low Voltage	V_{OL}	I_{OL} = 1 mA			0.2	V
Outputs						
POK High State Leakage	IL	V_O = 12 V		0.01	1	µA
POK Low Voltage	V_{OL}	I_{OL} = 10 mA			0.2	V
FAULT High State Leakage	I_L	V_O = 12 V		0.01	1	µA
FAULT Low Voltage	V_{OL}	I_{OL} = 10 mA			0.2	V
CBD (Crow Bar Drive) Minimum Output Current	I_{OH}	V_{CC} = 12 V, V_{OH} = 9 V	–40	–70		mA
CBD Output High Voltage	V_{OH}	V_{CC} 12 V				
		I_{OH} = 40 mA	9.0			V
		I_{OH} = 0 mA	9.5			V
CBD Pulldown Resistance	R_{OUT}	I_{OL} = 1 mA	300	500	700	Ω
Start-Up Functions						
UVEN Pullup Current Source	I_{OH}	V_O = 0 V	–0.6	–1	–1.4	µA
UVEN Clamp	$V_{OH\,MAX}$			4.0	4.1	V
UVEN Pulldown	I_{OL}	V_O = 0.5 V	10			mA
UVEN Low Output Voltage	V_{OL}	I_O = 100 µA			0.2	V
PG CAP Pullup Current Source	I_{OH}	V_O = 0 V	–0.6	–1	–1.4	µA
PG CAP Clamp	$V_{OH\,MAX}$			4.0	4.1	V
PG CAP Pulldown	I_{OL}	V_O = 0.5 V	10			mA
PG CAP Low Output Voltage	V_{OL}	I_O = 100 µA			0.2	V

Electrical Characteristics (cont'd)

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are V_{CC} = 12 V; +3.3 V = 3.3 V; +5 V = 5V; +12 V = 12 V; −12 V = −12 V; −5 V = −5 V.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF Input High Voltage	V_{IH}				0.8	V
OFF Input Low Voltage	V_{IL}		2.0			V
OFF Pullup Current	I_B	$V_I = 0$ V		100	150	µA
Voltage Reference						
Output Voltage	V_{REF}	$I_{REF} = -1$ mA, $T_J = 25°$ C	3.283	3.300	3.317	V
Line Regulation	ΔV_{REF}	$V_{CC} = 5$ V to 15 V		10	15	mV
Load Regulation	ΔV_{REF}	$I_{REF} = 0$ V to −5 mA		10	15	mV
Temperature Deviation*	ΔV_{REF}	$0 < T_J < 105°$ C		10	15	mV
Error Amplifier						
Input Voltage (Internally Tied to 3.3 V)	V_{FB}	$T_J = 25°$ C	3.267	3.300	3.333	V
Offset Voltage (EA+ Option)	V_{OS}		−20	0	20	mV
Input Bias Current	I_B			−0.1	−1	µA
Voltage Gain	A_{VOL}	$2 \text{ V} < V_{COMP} < 4 \text{ V}$	65	90		dB
Transconductance	gm			1		mA/mV
Unity Gain Bandwidth[1]	GBW		0.8	1.2	1.6	MHz
Power Supply Rejection Ratio	PSRR	$12 \text{ V} < V_{CC} < 20 \text{ V}$	60	70		dB
Output Sink Current	I_{OL}	$V_{FB} = 3.6$ V, COMP = 1.5 V	10			mA
Output Source Current	I_{OH}	$V_{FB} = 3.0$ V, COMP = 5 V	−0.6	−1.0		mA
Output Swing High	V_{OH}	$V_{FB} = 3.0$ V, $R_L = 15$ kΩ, $V_{CC} = 12$ V	9			V
Output Swing Low	V_{OL}	$V_{FB} = 3.6$ V, $I_{OL} = 350$ µA		0.7	1.1	V

*Temperature deviation is defined as the maximum deviation of the reference over the given temperature range and does not imply an incremental deviation at any given temperature.

PROPOSED

Typical Performance Curves

Not Available at Time of Publishing

PROPOSED

Package Dimensions

All Dimensions in mm (inches)

Not Available at Time of Publishing

PROPOSED

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ASTEC

AS17xx

Semicustom Bipolar Array

Features

Size (single tile)

- 87 x 75 mils
  Expandability of array
  (to 2 or 4 tiles)

Component Availability (single tile)

• Small NPN	48
• Dual collector PNP	21
• Vertical PNP	4
• Power NPN	3
• Diffused Resistors (total)	≈300 kΩ
• Pinch Resistors (3-terminal, 30kΩ)	8
• Cross-unders	13
• Buses	6

Basic Electrical Specs

• Transistor Matching (NPN & PNP)	<2%
• Primary voltage limitations:	
LV_{CEO}	18 V
BV_{CBO}	30 V
• Diffusion to substrate (Ground)	30 V
• NPN Parameters	
Beta	80–500
f_T (1mA)	300 MHz
BV_{EBO}	7 V
• PNP Parameters:	
Beta	20–300
f_T (1mA)	300 MHz
BV_{EBO}	30 V

Description

The AS17xx is Astec's proprietary semicustom bipolar array. This semicustom IC is a collection of individual transistors and resistors in a fixed configuration. The custom circuit is manufactured by creating a single metal mask to connect the components. This allows the designer to deal with only one mask for the IC layout instead of the actual 10 mask process. The semicustom array is useful for a wide range of functions, both analog and digital. In its simplest configuration, the AS17xx has 76 active devices available, but can be expanded to give up to four times this number in its largest configuration. This expandability of the array is a unique feature, allowing a whole range of semicustom circuits to be manufactured.

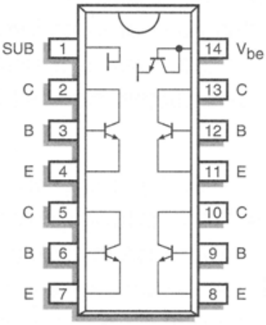
Because Astec has ongoing manufacturing of high volume circuits on this array, incremental wafer costs for engineering purposes are low. Therefore quality and reliability can be maintained even with small volume or engineering lots. Since the silicon can be completely processed and held awaiting only the metal etch and passivation steps, extremely fast turn-around times can be achieved.

The AS17xx bipolar array uses a standard "20 Volt" bipolar technology. Although quite similar to industry standard arrays, it has a number of important improvements. First, the ratio of PNPs to NPNs has been increased to allow for more modern design practice. Second, the process has been modified to allow for a deep collector diffusion (sinker) which not only improves the $V_{CE(SAT)}$ of the transistors, but also allows for the elimination of regions with thin oxide which historically plague semicustom die with electrostatic discharge reliability concerns. Third, a set of low resistance sinker resistors allows for bussing supply or signal lines without using active components for cross-unders. In addition, the specific component geometries have been further optimized to facilitate the layout compared to the industry standard arrays. Resistors are now in a binary weighted 500 / 1k / 2k / 4k sequence for more simple value calculations. The power devices use multiple standard size emitters so that they may also be used to create a device with an integral emitter area ratio with respect to a standard small NPN.

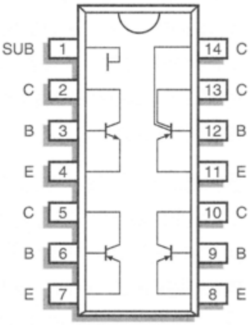
The AS17xx bipolar array can be packaged in industry standard DIP or surface mount packages with 8 to 40 leads. The number of pads available on the AS17xx varies with the number of tiles used as follows: single tile per die = 18 pads, two tiles per die = 30 pads, and four tiles per die = 40 pads. The extra pads not used for bonding to leads can be used for wafer level testing, trimming, and debugging.

Pin Configuration — Top view

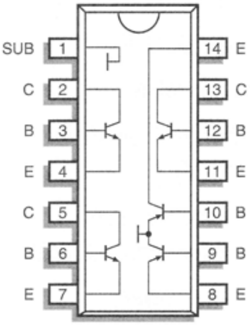
PDIP (N)
AS1700-NPN Kit Part



PDIP (N)
AS1700-PNP Kit Part



PDIP (N)
AS1700-PWR Kit Part



Die Configuration — Top view

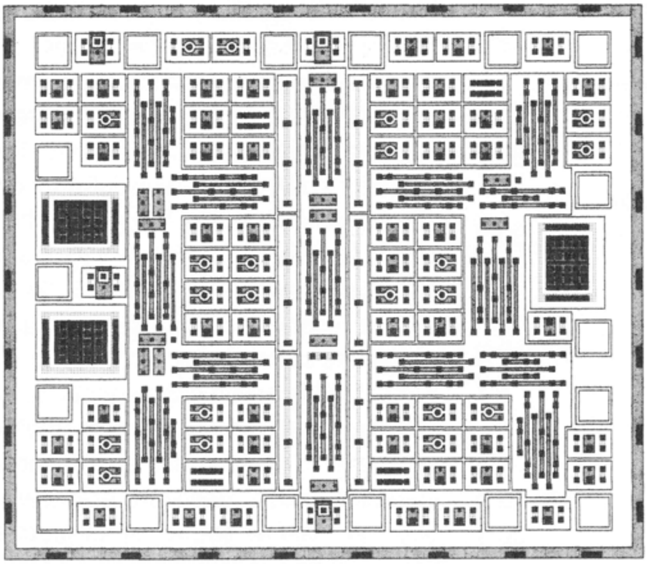


Figure 1. Single Tile Bipolar Array

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Continuos Power Dissipated at 25° C	P_D		
Single Transistor		300	mW
Total Package		1400	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	–65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

All parameters measured at 25° C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AS1700-NPN: Minimum NPN						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	I_C = 1 mA	20	35		V
Collector-to-Base Breakdown Voltage	BV_{CBO}	I_C = 100 µA	50	60		V
Emitter-to-Base Breakdown Voltage	BV_{EBO}	I_E = 10 µA	5	8		V
Collector Cutoff Current	I_{CEO}	V_{CE} = 18 V	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 10 µA, I_C = 100 µA	0	95	200	mV
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 100 µA	650	680	700	mV
Static Forward Current-Transfer Ratio	β (h_{FE})	V_{CE} = 3 V, I_C = 100 µA	80	125	500	
Early Voltage	V_A			–150		V
Transistor Matching (measuring ΔI_C)		I_C = 200 µA	–10	<1	10	%
AS1700-PWR: Large NPN (20-emitter)						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	I_C = 1 mA	20	35		V
Collector-to-Base Breakdown Voltage	BV_{CBO}	I_C = 100 µA	50	58		V
Emitter-to-Base Breakdown Voltage	BV_{EBO}	I_E = 10 µA	5	7.6		V
Collector Cutoff Current	I_{CEO}	V_{CE} = 18 V	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 200 µA, I_C = 2 mA	0	20	200	mV
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 200 µA	650	680	700	mV
Static Forward Current-Transfer Ratio	β (h_{FE})	V_{CE} = 3 V, I_C = 2 mA	80	125	500	
Early Voltage	V_A			–150		V

Electrical Characteristics (cont'd)

All parameters measured at 25° C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AS1700-PNP: Lateral PNP						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	$I_E = 100\ \mu A$	30	50		V
Field-Effect Threshold Voltage	VTF	$I_E = 10\ \mu A$		36		V
P + to Substrate Leakage	I_{SUB}	$I_E = 100\ \mu A$, $V_B = 1\ V$	0	150	500	nA
Collector Cutoff Current	I_{CEO}	$V_{CE} = 18\ V$	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	$I_B = 10\ \mu A$, $I_E = 100\ \mu A$	0	150	200	mV
Base-to-Emitter Voltage	V_{EB}	$V_{EC} = 3\ V$, $I_E = 100\ \mu A$	630	690	700	mV
Static Forward Current-Transfer Ratio	$\beta\ (h_{FE})$	$V_{EC} = 3\ V$, $I_E = 100\ \mu A$	20	60	300	
Early Voltage	V_A			–105		V
Transistor Matching (measuring ΔI_E)		$I_E = 200\ \mu A$	–10	<1	10	%
Double Collector Matching (meas. ΔI_E)		$I_E = 200\ \mu A$	–10	<1	10	%
AS1700-PWR: Vertical PNP						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	$I_E = 100\ \mu A$	30	50		V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 18\ V$	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	$I_B = 10\ \mu A$, $I_E = 100\ \mu A$	0	150	200	mV
Base-to-Emitter Voltage	V_{EB}	$V_{EC} = 3\ V$, $I_E = 100\ \mu A$	650	680	700	mV
Static Forward Current-Transfer Ratio	$\beta\ (h_{FE})$	$V_{EC} = 3\ V$, $I_E = 100\ \mu A$	20	125	500	

Typical Performance Curves

Minimum NPN

BETA vs I_C Over Temperature (−55° C to 125° C)

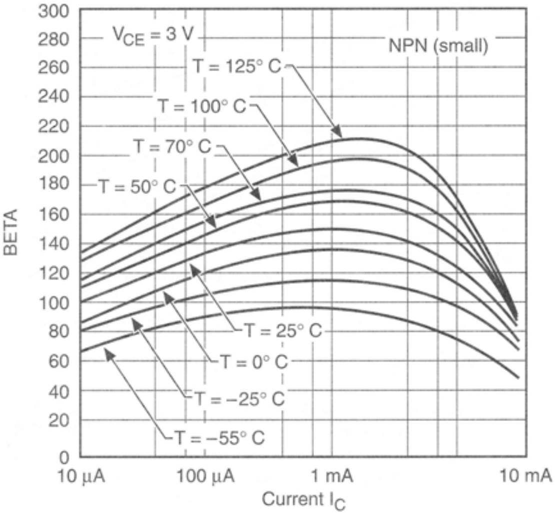


Figure 19

V_{EBO} Breakdown Voltage vs Temperature

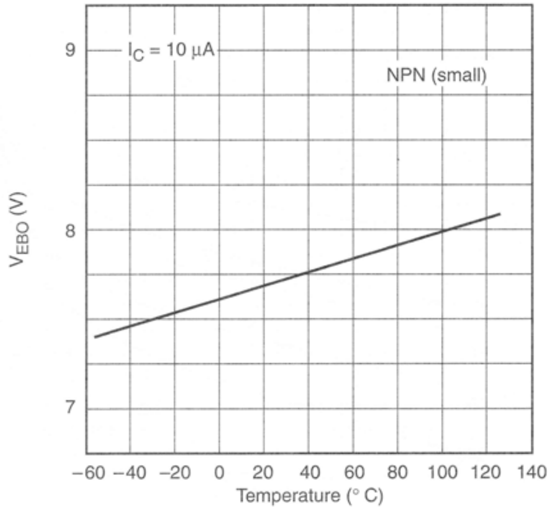


Figure 20

$V_{CE\ SAT}$ vs I_C Over Temperature (−55° C to 125° C)

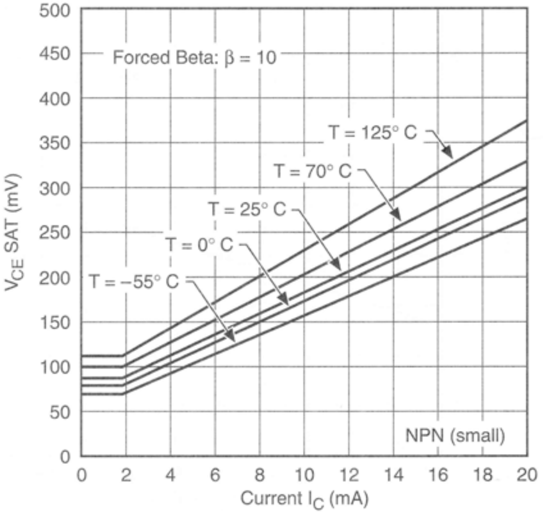


Figure 21

$V_{BE\ SAT}$ vs I_C Over Temperature (−55° C to 125° C)

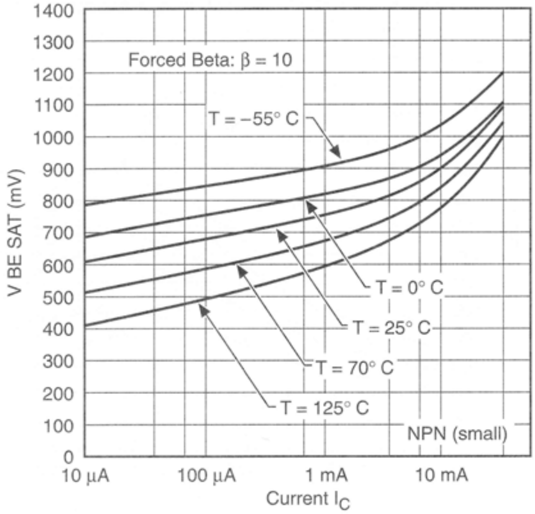


Figure 22

Typical Performance Curves

V_{BE} vs I_C Over Temperature (–55° C to 125° C)

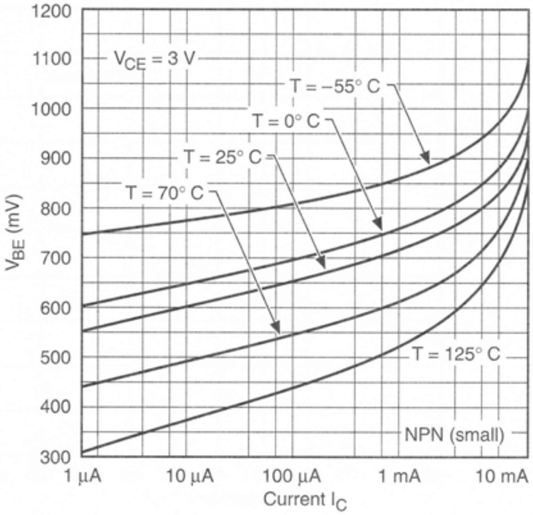


Figure 23

V_{BE} vs Temperature with Different I_C

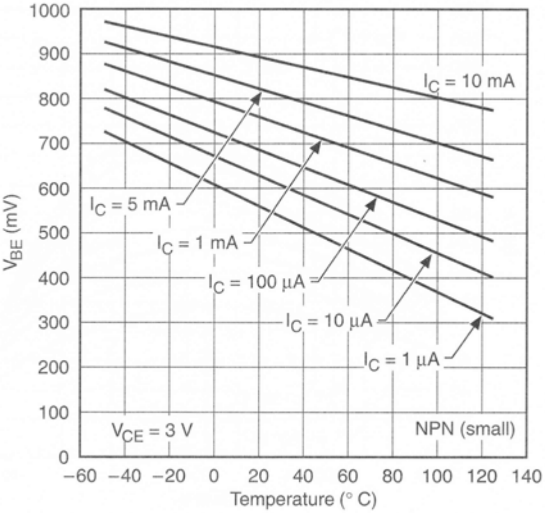


Figure 24

BETA vs I_C Over Temperature (–55° C to 125° C)

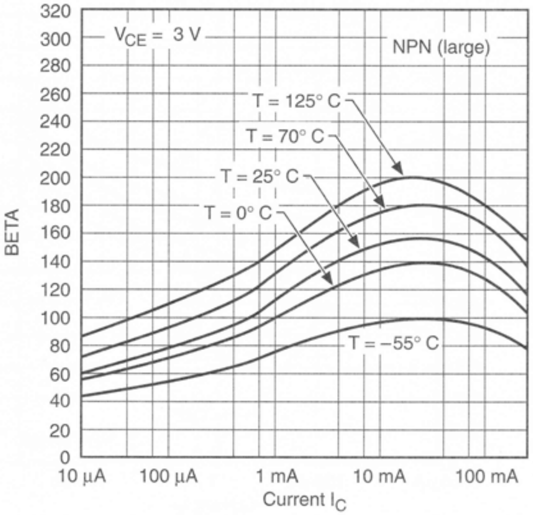


Figure 25

V_{EBO} Breakdown Voltage vs Temperature

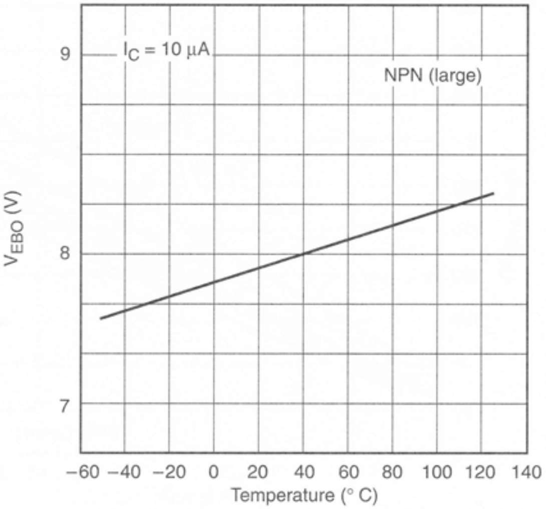


Figure 26

Typical Performance Curves

$V_{CE\ SAT}$ vs I_C Over Temperature (−55° C to 125° C)

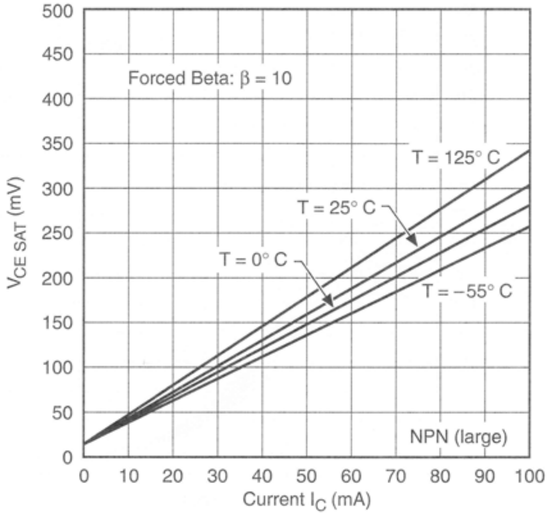


Figure 27

$V_{BE\ SAT}$ vs I_C Over Temperature (−55° C to 125° C)

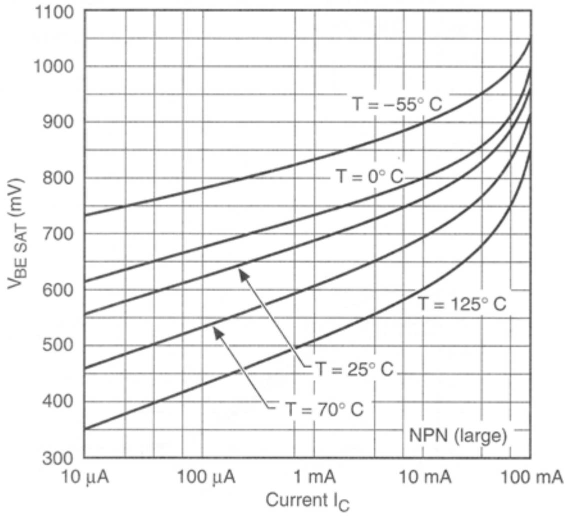


Figure 28

V_{BE} vs I_C Over Temperature (−55° C to 125° C)

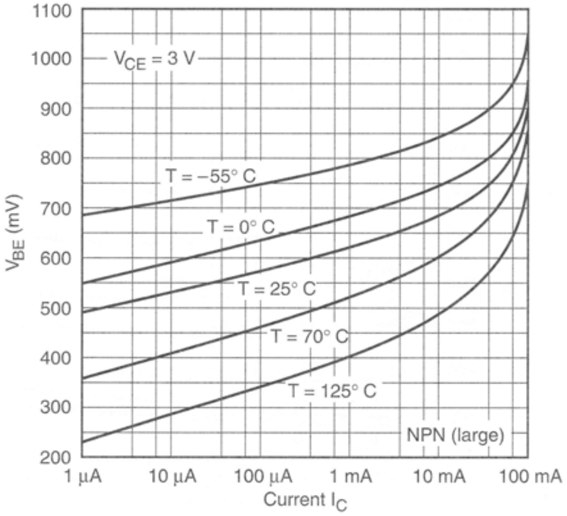


Figure 29

V_{BE} vs Temperature with Different I_C

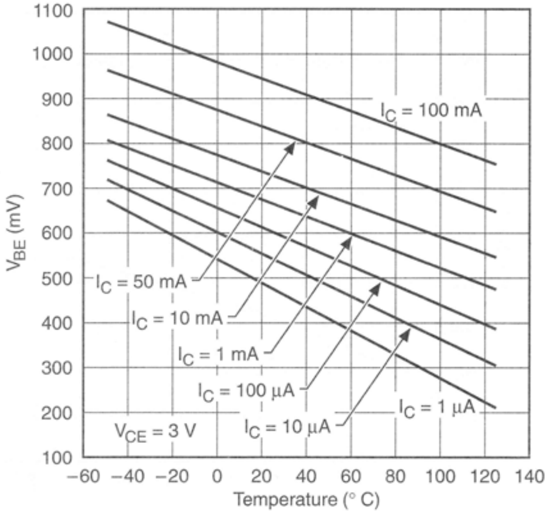
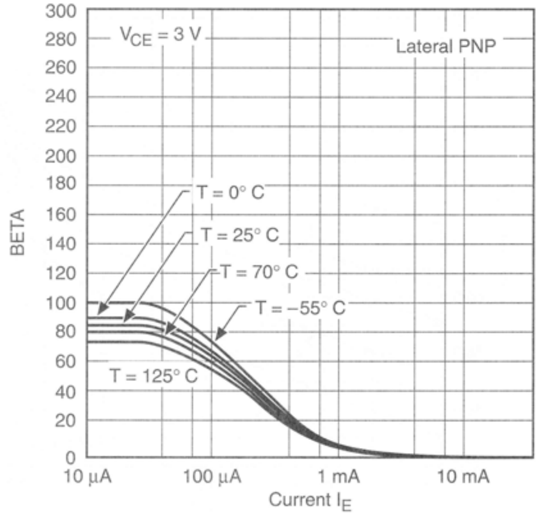


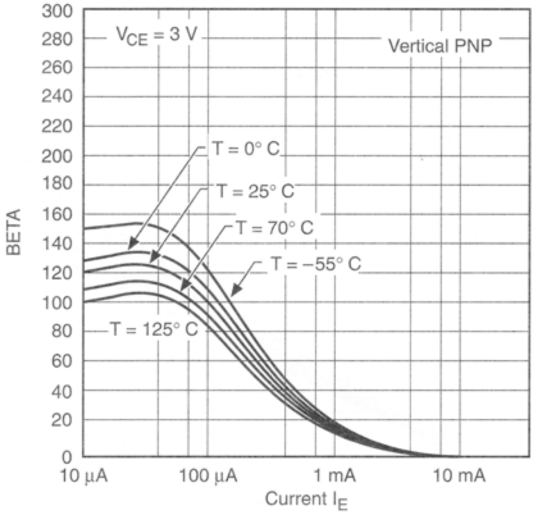
Figure 30

Typical Performance Curves



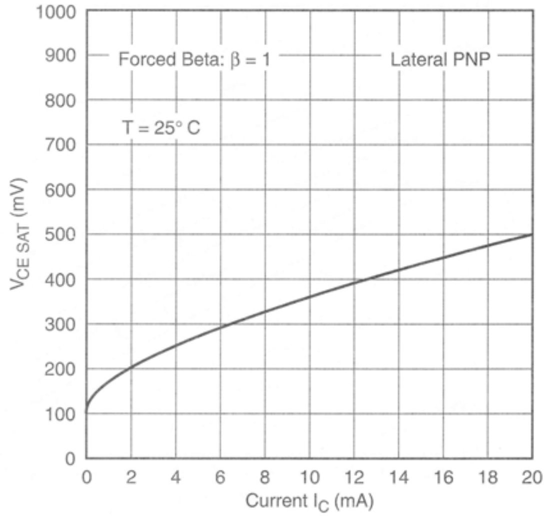
BETA vs I_E Over Temperature (−55° C to 125° C)

Figure 31



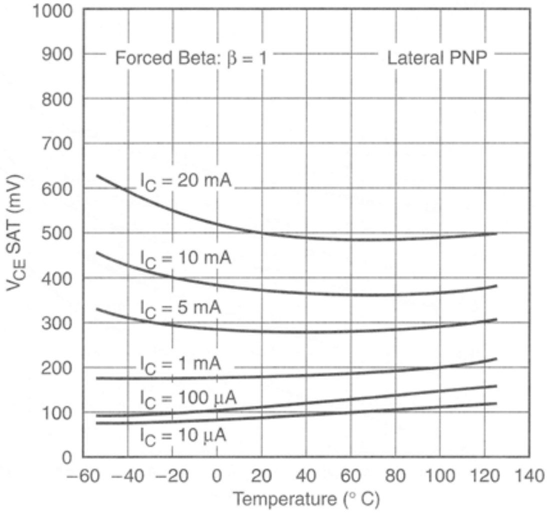
BETA vs I_E Over Temperature (−55° C to 125° C)

Figure 32



$V_{CE\ SAT}$ vs I_C

Figure 33



$V_{BE\ SAT}$ vs Temperature (With different I_C)

Figure 34

Typical Performance Curves

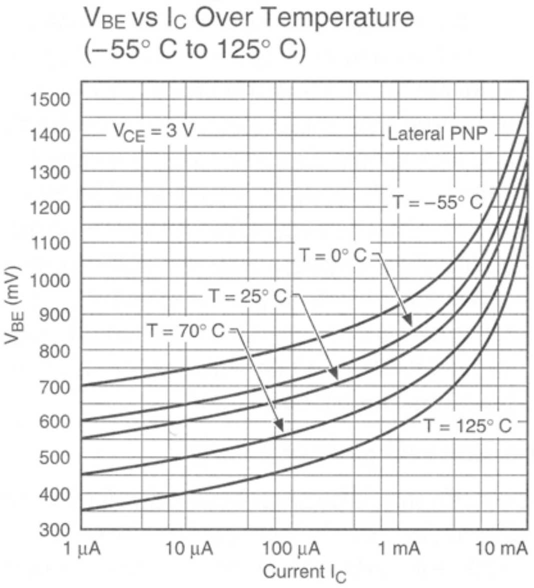

V_{BE} vs I_C Over Temperature (−55° C to 125° C)

Figure 35

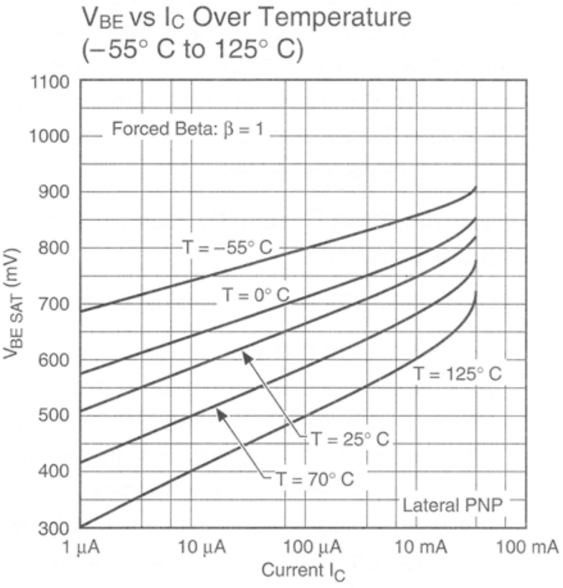

V_{BE} vs I_C Over Temperature (−55° C to 125° C)

Figure 36

The Semicustom Application

The Design Considerations

The designer should take advantage of the resistor and transistor matching available with ICs and not rely on the absolute values of parameters. If a certain emitter area is desired for current ratioing, several transistors can be connected in parallel to simulate this condition, or by using the desired emitter area of an NPN power device (when breadboarding use the previous method). When using the double-collector PNP transistors, do not float one of the collectors; either tie them together or tie one to the substrate. Floating one of the collectors, will severely reduce the beta. There are several values and types of resistors available on the AS17xx semicustom array as outlined in the resistor summary.

Resistor Summary

8 - Pinch Resistors
(≈30 kΩ ± 50%, use at ≤ 5 V)
80 - Base String Resistors
Using full string lengths gives:
73 – 4 kΩ
7 – 1.5 kΩ
Using separate pieces of the strings gives:
67 – 500 Ω
63 – 1 kΩ
43 – 2 kΩ
30 – 4 kΩ

Note: Don't try to use one resistor string for more than one resistor unless they are connected together in the circuit.

Additional components and their resistances are as follows:

13 - Cross-unders (370 Ω for full length, and 190 Ω for half length)
6 - Buses (at 10 Ω between connection points)

Non-Integratable Components

Identify all non-integratable components such as inductors and capacitors. These will have to be supplied with external components. Note that junction capacitors can be formed using transistors with collector and emitter tied together for limited capacitance values.

Minimizing Stray Effects (Parasitics, Currents, and Capacitance)

The following steps are recommended:

1) Try to keep substrate currents as low as possible (under a few mA) to prevent isolation loss and cross-talk between adjacent components. If a component has a high substrate current, try to isolate it from the other components and keep it as close to the substrate bonding pad as possible. The substrate current should be measured for either each kit part or the whole breadboard (with all the substrates tied together) using a 10 Ω resistor connected to the most negative potential in the circuit.
2) Do not saturate any PNP. If this is unavoidable, limit the base current so that the substrate current in the kit part lead is kept low. This is because of the parasitic vertical PNP formed between the emitter, base and substrate in a lateral PNP will become active when the lateral PNP is saturated.
3) Do not use any diode-connected PNP over about 500µA to avoid the above mentioned parasitic PNP.
4) Contact the N-layer (collector-plug) in the resistor-tubs to the most positive potential (this is for resistor-tub biasing and isolation, and is a concern only for the semicustom implementation of the circuit), and the substrate to the most negative potential in the circuit.
5) High-frequency oscillations can, on rare occasions, occur in the integrated circuit when the breadboard did not show any tendency toward oscillation. This can be caused by the stray capacitances in the breadboard, which are larger than those associated with the IC and tend to stabilize potentially unstable circuits. Therefore, every effort should be made to minimize stray capacitances in the breadboard. This can be done by using DIP sockets and soldered wire or printed circuit interconnects rather than the popular solderless plug-in breadboards which have up to 10pF of pin-to-pin capacitance.

Breadboarding with Kit Parts

All circuits should be breadboarded before being implemented on the semicustom array using AS1700 Kit Parts, (which are transistor arrays made using the AS17xx semicustom array). This breadboard will simulate as accurately as possible all stray effects and how the circuit will perform when implemented with the semicustom array. We recommend that standard carbon resistors be used to simulate the integrated resistors, or precision thin film resistors if accurate ratios are required.

Evaluating your breadboard

After obtaining satisfactory performance from the breadboard, evaluate the effects of resistor, transistor and temperature variations.

We recommend simulating the worst-case resistance variations (which is 30% globally and 1% for matching and ratioing) on the breadboard by substituting the appropriate values for all resistors. Sensitivity to transistor parameter variations can be seen by interchanging kit parts. We also recommend that the breadboard be tested over the full operating temperature range of the circuit.

After testing is complete, make sure that the breadboard circuit is accurately reflected in the schematic by doing a thorough check to see if all modifications to the breadboard are included.

Layout options

After thoroughly testing the breadboard, begin the layout process. There are three options for doing the layout:

- **Customer layout** - You do the layout and provide Astec with a completed layout sheet (at 500x - which Astec will provide) ready for entry into our CAD system. Astec will review the layout for design rule violations and advise you so that you can correct them yourself or elect to have Astec fix them.
- **Vendor layout** - You may assign Astec the responsibility of the IC layout.
- **Customer supervised layout** - You assign the layout implementation to Astec but retain the responsibility for the final form and content. Basically you are subcontracting Astec to do the IC layout under your direction. This option requires a great deal of communication between the customer and Astec, but can yield the greatest control for the customer while reducing the layout time.

Layout guidelines

We recommend that several copies of the layout on the data sheet be made to facilitate the layout process before working with the 500x layout sheet. The layout copies can be used to sketch various interconnect options, and work out any design problems that may be incountered because of the layout process.

Functional blocks: We recommend that the circuit be broken down into functional blocks. The blocks are selected in such a way as to minimize the the number of interconnections with the other blocks. If the blocks are in sequence, the circuit can usually be divided so that only one or two connections are made between the blocks (other than power supply connections).

Block location: Next, add up the number of devices and pads required by each block. Then select an area of the chip for each block. There are a few considerations which must be kept in mind for the block placement. First, the selected area must contain the required number of components and pads. Second, the various areas should be located so that interconnections between them are as easy as possible. Finally, the locations of the various pads to be bonded to pins and their relationships to each other and the blocks should be considered. Bond wires should not cross each other.

Cross-unders & buses: Cross-unders can be useful for small resistance values, but be careful of connections that can not tolerate cross-under resistance (see resistor summary), such as the base connections for a diode-biased current source, etc. To make sure that a connection can tolerate the cross-under resistance, insert the appropriate valued resistor in the breadboard and evaluate its effect on circuit performance. Buses have low resistance and are valuable for connecting functional blocks together, and busing power supply voltages.

Thermal considerations: If one or more components dissipate heat, they should be located away from other components that require close matching. The matched components should be placed together an equal distance from the thermal source. This way both of the matched components will be heated equally. Total power dissipation in the circuit is a function of the package type and size. On average at least 500 mW can be dissipated without trouble. Larger packages can dissipate more heat.

Signal & common coupling: If high frequency signals are present which have large amplitude swings, these lines should be separated as much as possible with respect to their pin locations because of inductive or capacitive coupling between their pins and bonding wires.

Another coupling problem arises when there are long metal lines. For example, if there is a common ground line for both the input and output of an amplifier, the fluctuating current from the output could cause a voltage drop along the line that could effect the input. This coupling could cause distortion or oscillations. The solution to this problem is to run two separate ground lines to the ground pad.

Resistor ratioing: Where matched resistor values or precise ratios are required, identical resistor constructs and orientations should be used. Identical resistors orientated 90° to each other may have different values due to directionally dependent fabrication and packaging tolerances.

Component interconnection: We recommend numbering the components on the circuit schematic and using these numbers on the layout. Work on only one circuit block at a time and leave the block interconnections until all the blocks are finished. Start the layout by selecting several components of a block and placing them on the layout; sketch their interconnections and work outward marking the schematic as you go.

Metal routing: The metal routing can be sketched on the layout sheet taking into account the design rule considerations as follows:

Design Rules:

- Minimum metal width = 8 microns
- Minimum spacing between metal traces = 8 microns
- Current capacity of metal trace = 4 mA per micron of width
- Metal line to pad (active) = 24 microns (note: metal resistance ≈ 0.02 Ω per square)

The area around the outside of the chip has a metalized ring with numerous contacts to the substrate. The substrate must be connected to the most negative potential in the circuit. When laying out the circuit, the ground conductors should lead inward from the outer ring. There are several N-layer contacts for the different resistor tub areas that must be connected to the most positive potential in the circuit to maintain isolation.

Bonding pads: The rules for bonding pad layouts are very simple. You must be able to draw a straight line from a bonding pad to its pin without crossing any other wires, and the pads should be evenly spaced around the chip. The pin assignments are arbitrary, but they should be organized such that the pin numbers correspond to the pads in a counter-clockwise rotation around the chip, and not some random pattern that would cause bonding wires to cross each other.

Layout sheets (500x) are available upon request for final layout, and are used to make the metal interconnect mask and check spacing rules. We recommend that the metal interconnect be done on a clear film over the layout sheet with erasable markers before making the final layout. This will allow for modifications to be made with a minimum amount of effort.

Functional Circuit Blocks

The following circuits are presented as a guide to assist in circuit design using the AS17xx Semicustom Array.Complex circuit functions can created from these elementry building blocks.These circuit blocks can be modified and improved to suit the designer's needs in creating a complete system.

Current Sources

Here are a few examples of PNP current sources; NPN current sinks can easly be derived from the analog of these PNP examples.

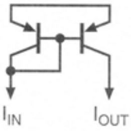


Figure 2. Simple PNP Current Source. Has Slower Frequency Response, and up to ±15% Tolerance Error.
$I_{OUT} = I_{IN} * (1 + 2/\beta)$

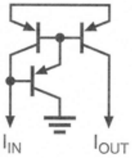


Figure 3. Widlar Current Source, Moderate Frequency Response.
$I_{OUT} = I_{IN} * (1 + 2/\beta^2)$

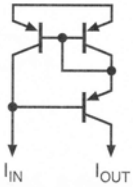


Figure 4. Wilson Current Source, Fast Frequency Response.
$I_{OUT} = I_{IN} * (1 + 1/2\beta^2)$

Comparator Input Stages

Several comparator input stages are illustrated below.

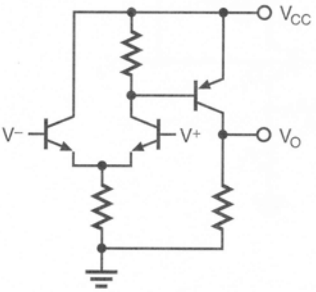


Figure 5. Simple NPN Type Comparator.

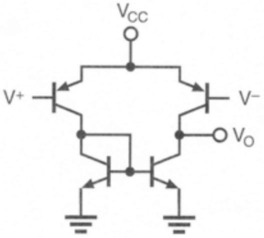


Figure 6. Simple NPN Type Comparator Input Stage.

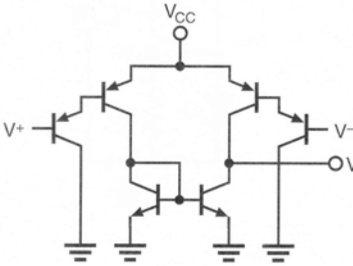
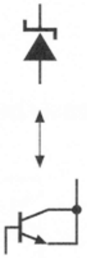


Figure 7. Improved PNP Yype (Good GND Sensing) Comparator Input Stage.

Functional Circuit Blocks

Voltage Regulators/References



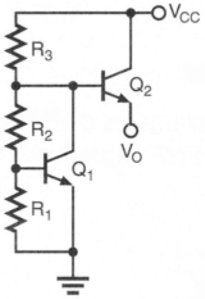
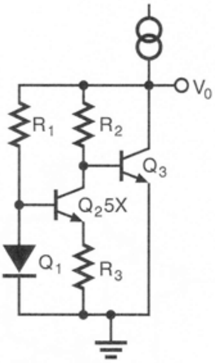


Figure 8. Zener Diode $V_Z = 7$ V

Figure 9. V_{BE} Multipled Regulator.
$V_{OUT} = V_{BE}(Q1) * (R2 + R1)/R1$



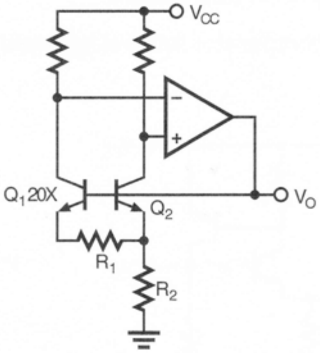


Figure 10. Widlar Band Gap Reference.
$\Delta V_{BE} = V(R3) = V_T * L_N (A2/A1)$ V_{OUT}
$= V_{BE}(Q1) = (R2/R3) * \Delta V_{BE}$

Figure 11. Brokaw Band Gap Reference.
$\Delta V_{BE} = V(R1) = V_T * L_N (A1/A2)$ V_{OUT}
$= V_{BE}(Q2) = V(R1) * 2 * R2/R1$

Functional Circuit Blocks

Flip-Flop

Here are two examples of flip-flop circuits.

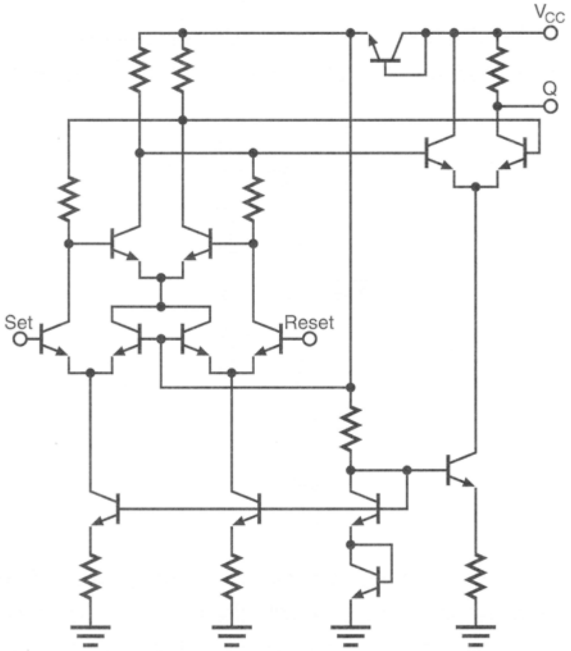


Figure 17. Fast, ECL Flip-Flop

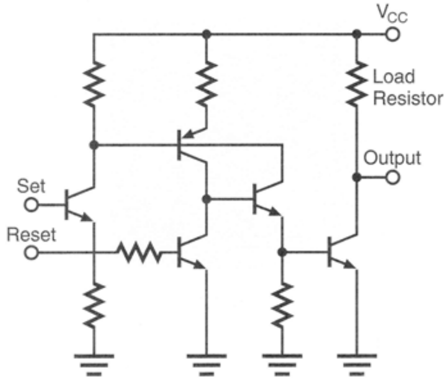


Figure 18. Four Layer Latch Flip-Flop

Functional Circuit Blocks

Trimming Schemes

There often arises the need to trim a parameter (i.e. voltage, current, oscillator frequency, offset null, etc.) to some particular value because of processing variations involved with wafer fabrication. We have developed two methods to accomplish this goal: 1) fuse link, where a fuse is blown to cause an open; and 2) zener zap, where a zener is taken well into breakdown until a short occurs.

Fuse Link

Fuse links can be used similar to zeners for trimming, but the fuses must be located on a bonding pad inside the pad cut because a fuse won't blow if there is passivation over it. One possible trim scheme using fuse links is shown below.

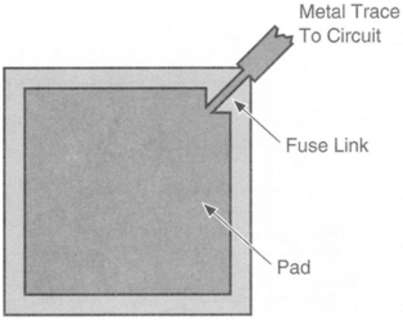


Figure 12.

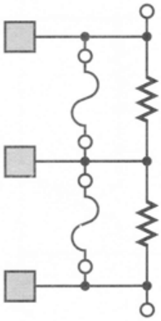


Figure 13.

Zener Zap

When using zener zap trim methods there are several points to keep in mind: the zener should be located near a pad, no cross-unders should be used to connect the zener with the pad, and the metal lines connecting the pad to the zener should be as thick as possible to allow the high current necessary to blow the zener. A few examples of the many possible trim schemes are shown in Figure 14, Figure 15 and Figure 16.

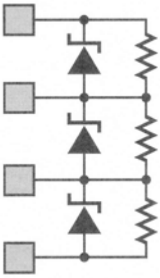


Figure 14. Simple Trim Setup with 8 Trim Steps.

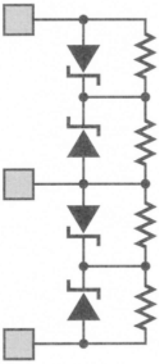


Figure 15. Trim Scheme Using Only 3 Pads to Get 16 Trim Steps.

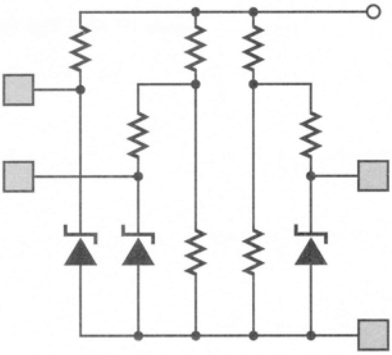


Figure 16. Parallel Trim Scheme with 8 Trim Steps.

Spice Models:

```
.MODEL Nmin NPN; Minimum NPN
   + (IS = 0.5FA  BF = 200  NF = .995  VAF = 100  IKF = 20M  NE = 1.45
   + EG = 1.185 BR = 5 NR = 0.98 VAR = 30 IKR = 2M XTB = 0.3
   + RB = 270 RC = 60 RE = 7 TRB1 = 1.5M XTI = 2.5
   + CJE = 450FF VJE = 0.85 MJE = 0.36 TF = 300PS
   + CJC = 200FF VJC = 0.57 MJC = 0.47
   + CJS = 1.4PF VJS = 0.31 MJS = 0.35)
.MODEL Plat LPNP; Lateral PNP
   + (IS = 0.9FA BF = 80 NF = 1 IKF = 60U NE = 1.5
   + EG = 1.2 BR = 30 NR = 0.98 IKR = 2M
   + RB = 30 RC = 200 RE = 15 TRC1 = 1.5M TRE1 = 1.5M
   + VAF = 45 VAR = 30
   + CJE = 150FF VJE = 0.57 MJE = 0.47 TF = 30NS
   + CJC = 950FF VJC = 0.57 MJC = 0.47 XTB = 0.5
   + CJS = 1.4PF VJS = 0.31 MJS = 0.35)
.MODEL Pvert LPNP; Vertical PNP
   + (IS = 0.9FA BF = 100 NF = .995 VAF = 45 IKF = 1.5M
   + EG = 1.22 BR = 30 NR = 0.98 VAR = 30 IKR = 2M NE = 1.25
   + RB = 350 RC = 200 RE = 300 TRC1 = 1.5M TRE1 = 1.5M
   + CJE = 150FF VJE = 0.57 MJE = 0.47 TF = 30NS
   + CJC = 1.6PF VJC = 0.57 MJC = 0.47 XTB = 0.5)
.MODEL RBase RES; Base Resistor
   + (R = 1 TC1 = 2.1m TC2 = 7u)
.MODEL RImp RES; Implant Resistor
   + (R = 1.0 TC1 = 4m TC2 = 6u)
.MODEL RPinch RES; Pinch Resistor
   + (R = 1.0 TC1 = 7m)
.MODEL Dzener D;
   + (BV = 7.2V IBV = 1uA RS = 270 IS = .1fA)
```

Component Summary

Components Available (single tile):

Small NPN:	48
Dual collector PNP:	21
Vertical PNP	4
Power NPN	3
Diffused Resistors (total)	≈300 kΩ
Pinch Resistors (3-terminal, 30kΩ)	8
Cross-unders	13
Buses	6

Resistor Summary

Resistor Summary:

8 - Pinch Resistors
(≈30 kΩ ± 50%, use at ≤ 5 V)
80 - Base String Resistors
Using full string lengths gives:
73 - 4 kΩ
7 - 1.5 kΩ
Using separate pieces of the strings gives:
67 - 500 Ω
63 - 1 kΩ
43 - 2 kΩ
30 - 4 kΩ

Additional components and their resistances are as follows:

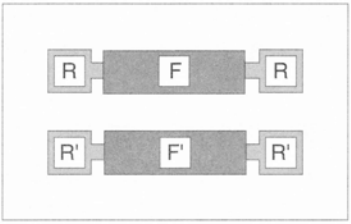
13 - Cross-unders (370 Ω for full length, and 190 Ω for half length)
6 - Buses (at 10 Ω between connection points)

Design Rules

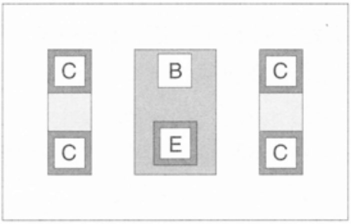
Design Rules:

- Minimum metal width = 8 microns
- Minimum spacing between metal traces = 8 microns
- Current capacity of metal trace = 4 mA per micron of width
- Metal line to pad (active) = 24 microns (note: metal resistance ≈ 0.02 Ω per square)

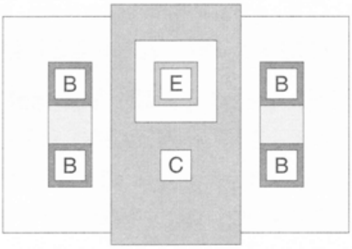
Device Layout



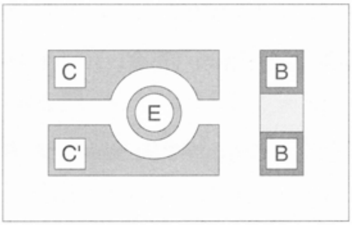
Pinch Resistor with Field Contact



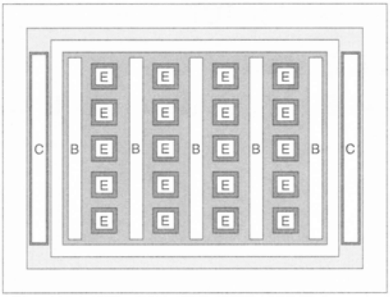
Minimum NPN



Vertical PNP

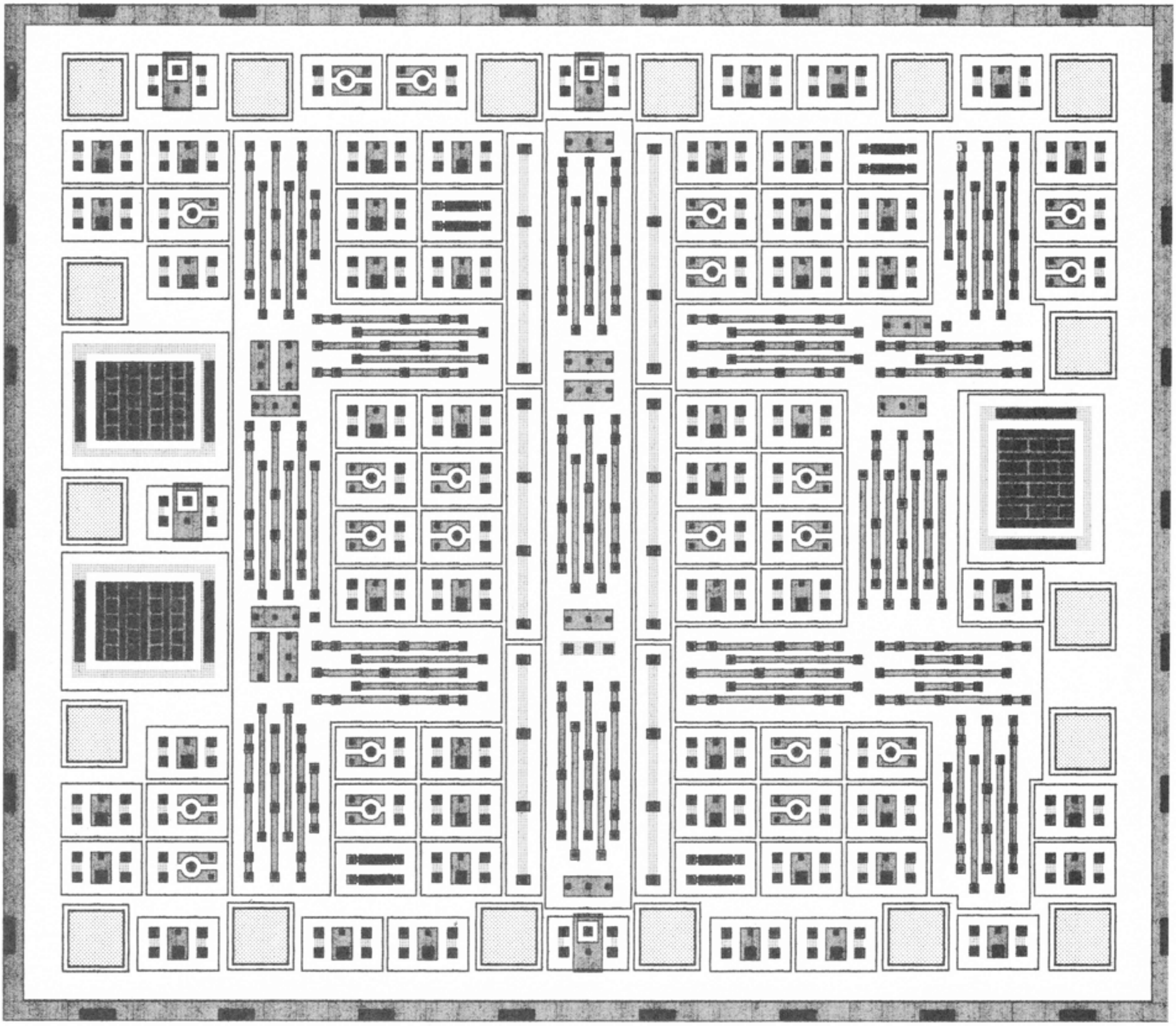


Lateral PNP with Split Collector



Power (20x) NPN

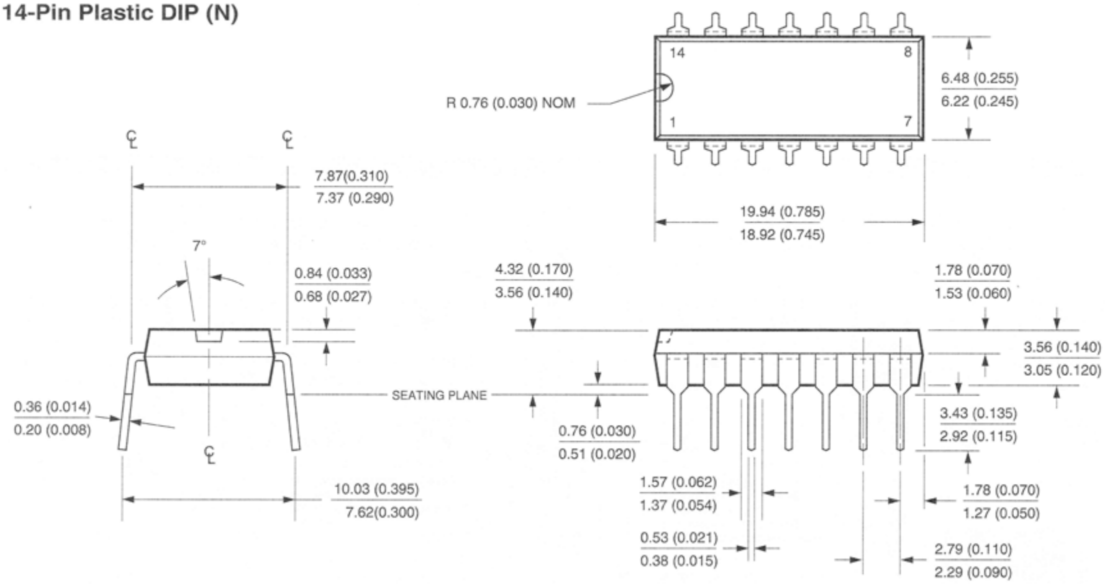
Device Layout



Package Dimensions

All Dimensions in mm (Inches)

14-Pin Plastic DIP (N)



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Application Notes

Application Note Cross-Reference

Product	Application Note
AS431	AN -1, AN - 2, AN - 5
AS1012	AN - 5
AS1200	AN - 3
AS384x	AN - 2, AN - 3, AN - 4, AN - 6

ASTEC

AS431
Application Note 1

General Application Information

Steve Contreras

The ASTEC AS431 is a low-cost Precision Temperature Compensated Reference IC that is well-suited for many applications in linear and power electronics. A direct replacement for the industry standard TL431, this IC offers improved AC performance, near zero Temperature Coeficient (TC), trimmed 0.5% tolerance and is available in a standard grades from 0 to 105° C and an extended temperature version, the AS1431, from –55 to 125° C.

When used with a minimum of external components, this device is ideal for a wide variety of applications including precision programmable voltage references, high speed amplifiers, comparators, linear series or shunt regulators, current sources or limiters, delay timers, voltage monitors, alarm circuits, and oscillators.

This application note demonstrates the versatility of the AS431 in typical applications and presents data useful for gaining a complete understanding of its application.

Figure 1 shows the schematic symbol and functional block diagram for the AS431. As indicated by the schematic symbol, the device can be thought of as a programmable zener diode. The functional block diagram, however, reveals a versatile IC consisting of a trimmed 2.5 V precision band gap reference, a high speed amplifier (Gain BW Product ≈ 3 MHz), ESD protection and a low impedance output stage. It is capable of shunting from 1 to 150 milliamps and has an output voltage range of 2.5 to 30 volts.

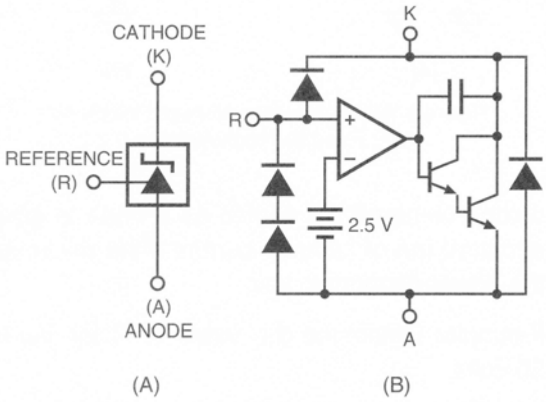


Figure 1. AS431 A) Schematic Symbol
B) Functional Block Diagram

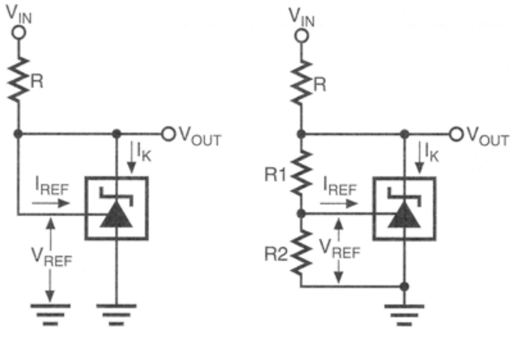
Typical Applications

Precision Voltage Reference

The most common application of the AS431 is a precision temperature compensated voltage reference as shown in Figure 2. Note that only one external resistor is required for an output voltage equal to V_{REF}. For output voltages other than V_{REF}, a simple resistor divider network is used.

Fixed 2.5 Volt Reference

For an output voltage equal to V_{REF}, the reference input pin is connected directly to the cathode. A single resistor R is used to set the cathode current (I_K). The value of R will depend primarily on Vin and the characteristics of the load impedance that the circuit output will see (similar to selecting the series resistor for an ordinary zener



(A) (B)

Figure 2. AS431 Precision Voltage Reference
A) Fixed B) Programmable

diode). Generally, R should be chosen to give about 10 mA of cathode current. This will keep the power dissipation low.

Example: Determine the value of R for V_{IN} = 20 volts.

The voltage across R is 20 – 2.5 = 17.5 V. For a desired I_K of 10 mA, R = 17.5/0.01 = 1.75 kΩ. Thus, an R of 1.8 kΩ will give an I_K of about 10 mA.

Programmable Output

To program the output to any desired value between V_{REF} and 30 volts, a simple resistor voltage divider is used as shown in Figure 2B.

V_{OUT} is determined by the formula:

$$V_{OUT} = V_{REF}\,(1 + R1/R2) + I_{REF} \bullet R1.$$

To ensure precise regulation, low TC precision 1% resistors should be used for R1 & R2. Its values should not be so low as to cause excessive power dissipation, nor too high that an error is introduced due to changes in I_{REF} over temperature (I_{REF} is typically 0.7 µA and deviates 0.4 µA over the full temperature range). A good compromise is to always keep R2 at around 2 to 5 kΩ and then select R1 to obtain the desired output voltage. The circuit can be made variable by using a potentiometer for R1.

The AS431 As An Error Amplifier

The AS431 can be used in both linear and switch mode power supplies as high gain error amplifier with a built-in temperature compensated voltage reference.

Linear Voltage Regulator

Figure 3 shows a simple linear voltage regulator. This circuit converts an unregulated DC source (rectified AC or battery) to a low-noise, low-ripple precision-regulated DC output. The output voltage can be set to any desired value between 2.5 to 28 volts, and the output current is limited only by the series pass element.

The high gain of the AS431 allows this circuit to achieve a line/load regulation of typically 0.03% or better, depending on the application.

Switch Mode Power Supply

The AS431 can be similarly used in switch mode power supplies as shown in Figure 4. The only difference is the AS431 does not control the

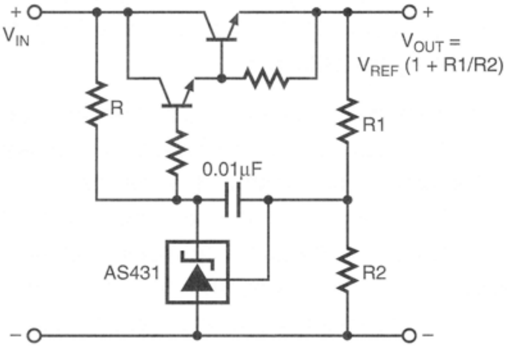


Figure 3. Linear Regulator Using the AS431 as a Reference/Error Amplifier

output voltage directly as in the linear regulator. Instead, it provides an amplified error signal to the PWM circuitry that in turn controls the on/off ratio of the switching device(s), thereby regulating the output voltage. Also, because of the phase shifts and delays associated with the modulator and filter components in switching power supplies, a more elaborate compensation network is required in the control loop to optimize the gain/phase characteristics of system. The network type and values are chosen so as to ensure stability and proper transient response.

Note that there are many different types of switching power supply topologies having different compensation, isolation and PWM configurations. The AS431 and associated circuitry, however, are essentially the same in all cases except for component values, the type of compensation network used and location (it may be located on the primary side in some applications).

The AS431 may also be used for other functions in a switch mode power supply. For example, it can be used as a reference or a comparator in the housekeeping, input/output monitoring, temperature control, or alarm circuitry. Or, as the reference/error amplifier in a MagAmp or linear auxiliary output regulator. Figure 6 illustrates several of these applications.

Frequency Compensation

Frequency compensation of a power supply control loop is achieved with an external compensation network, typically connected between the reference and cathode pins of the AS431. The type of network used can be as simple as a single capacitor, or as elaborate as a dual zero-pole pair network, depending on the power supply's topology. A typical single zero-pole pair compensation network is shown in Figures 4 and 5.

The AS431 typically has 55 dB of gain from DC to 6 kHz, where it rolls off at a 6 dB per octave rate, reaching 0 dB at 3 MHz. Further information characterizing the performance of the AS431 over frequency can be found in the AS431 Data Sheet. Due to the complexity of frequency compensation network design and the vast number of power supply topologies possible, a detailed discussion is beyond the scope of this application note. However, the information provided is useful in determining the compensation needed for a particular application.

The AS431 as a MagAmp Controller

Post regulation is required in many cases for one or more outputs of a switch-mode power supply. Linear regulators incorporating the AS431 are adequate for most low current outputs. When

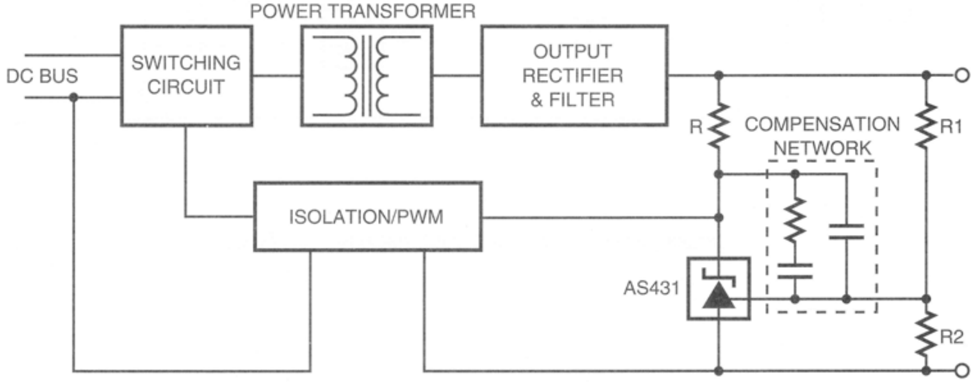


Figure 4. A Switch-Mode Power Supply Using the AS431 as a Reference/Error Amplifier

high current outputs are required, a MagAmp (saturable-core) regulator is usually used because of its high efficiency.

Generally speaking, a MagAmp is a pulse-width modulated buck regulator circuit that uses a saturable core inductor as the switching element. The inductor initially has a high inductance that blocks a pre-determined number of volt-seconds. Upon saturation, the inductor reverts to a very low impedance, which allows current to flow to the output with little loss. The number of volt-seconds blocked in each cycle is defined by the control circuitry and varies in accordance with changes in line and load, providing tight regulation at the output.

The AS431 is an ideal low-cost MagAmp controller, for it contains all the necessary control functions needed (precision reference, high gain error amplifier and an output stage) in a small package. A schematic diagram of a typical MagAmp post regulator using the AS431 is shown in Figure 5. Since this circuit constitutes a closed loop system, frequency compensation of the error amplifier is necessary.

Other Applications

The AS431 also can replace an ordinary zener diode in any circuit where a higher accuracy and temperature stability is required. Viewing the AS431 as a high gain transistor with a V_{BE} of 2.5 V increases usage possibilities. Applications for this device are limited only by the imagination.

Several practical applications are illustrated in Figure 6.

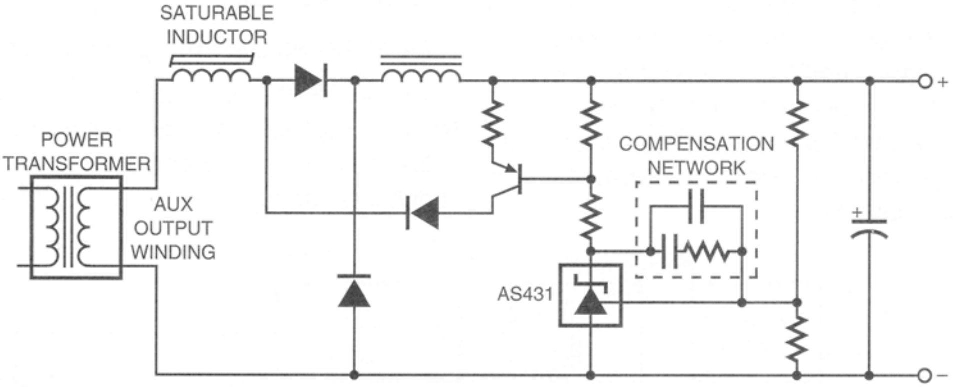
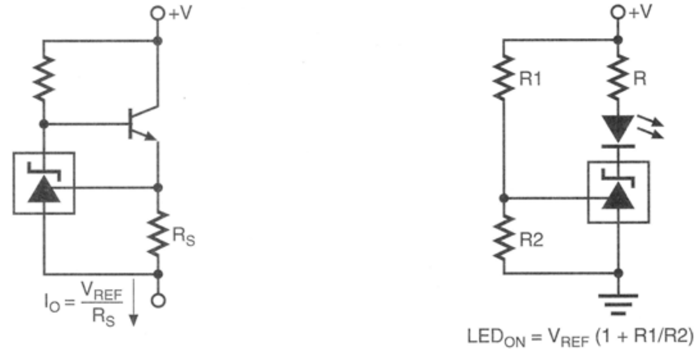


Figure 5. An AS431 Controlled MagAmp Post Regulator

CURRENT SOURCE

VOLTAGE MONITOR


+V
R_S
$I_O = \frac{V_{REF}}{R_S}$
+V
R1
R
R2
$LED_{ON} = V_{REF}\ (1 + R1/R2)$

COMPARATOR

CONSTANT CURRENT SINK

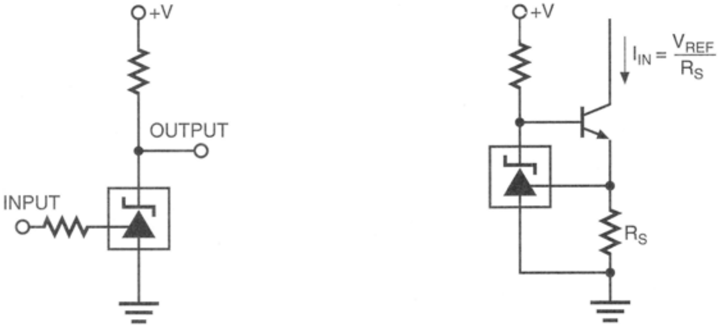


Figure 6. Typical AS431 Applications

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Notes

ASTEC

AS431
Application Note 2

Secondary Side Error Amplifier Using the AS431

Mike Wong

I. Introduction

One of the most important safety regulations to which an off-line power supply must conform is input to output electrical isolation. This isolation requirement prevents the power supply control IC from directly sensing both the input line and output voltages. In the case of primary side control the output regulation information, an error voltage, must be transferred from the secondary side. This application note discusses a simple way of transmitting regulation information across the electrical isolation using an AS431 and a conventional 4N27 opto-coupler.

II. Power Supply Circuit

Figure 1 illustrates a simple flyback regulator. The AS3842, a low-cost current mode control IC, is configured to regulate the power supply from the primary side. The AS431 acts as a reference and a feedback error amplifier to sense the output voltage and generate a corresponding error voltage. This error voltage is then converted to an error current and coupled to the primary side through a 4N27 opto-coupler.

III. Opto-Coupler

Recently, opto-coupler manufacturers have made major improvements in opto-coupler processing and packaging technologies, resulting in tighter current transfer ratio (CTR) tolerances and better long-term reliability.

When designing the opto-coupler feedback circuitry, the designer should note the opto-coupler forward diode current. The forward diode current sets the device's CTR and effects the long-term reliability of the device. Similar to a lamp filament,

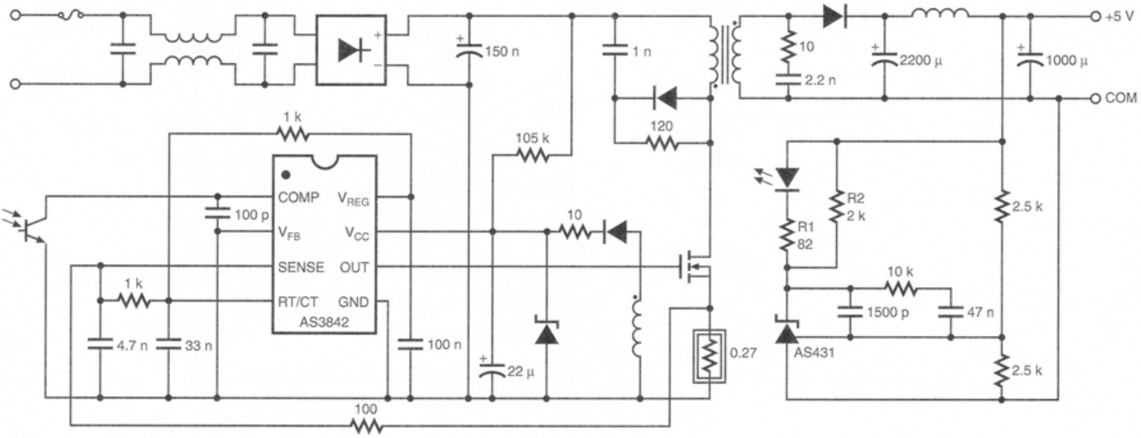


Figure 1. A 40W Flyback Power Regulator

the opto-coupler diode can be worn out or degraded more quickly if it is subjected to higher current. Also, the opto-coupler's unity gain bandwidth increases with forward diode current. The modulation of the gain bandwidth is caused by variations in the transconductance of the output transistor. In addition, the Miller capacitor from the base to collector of the output transistor damps out the effects of the opto-coupler's gain variance. A properly designed opto-coupler circuit not only increases long-term reliability of the regulator but also ensures a superior loop response.

IV. Design Example

Figure 2 shows the amplifier feedback section of the flyback power supply. To keep the 5 V output regulated, the V_{COMP} voltage must track the output voltage. The output voltage is first divided down by two 2.5 kΩ resistors, and its result is fed into an AS431 error amplifier network. The error amplifier output, $V_{CATHODE}$, is then converted to a proportional opto-coupler diode current. The opto-coupler bridges the isolation barrier and generates an output collector current proportional to the input diode current. Since the opto-coupler output is connected to the V_{COMP} pin, the opto-coupler output current is the I_{COMP} source current. In a normal operating condition, a higher output voltage causes $V_{CATHODE}$ to drop and results in a high diode current and I_{COMP} source current and consequently a lower V_{COMP}. A lower V_{COMP} decreases the PWM duty cycle and therefore decreases the regulator output voltage. The result is a regulated output. A determinination of the opto-coupler diode operating current and small signal loop gain follows.

IVa. Opto-Coupler Operating Current

This design example shows the diode operating current as determined by the maximum I_{COMP} source current. In order for V_{COMP} to decrease linearly with increasing I_{COMP} source current, I_{COMP} has to operate in a linear region slightly above the maximum I_{COMP} source current. The linear region is depicted in Figure 3.

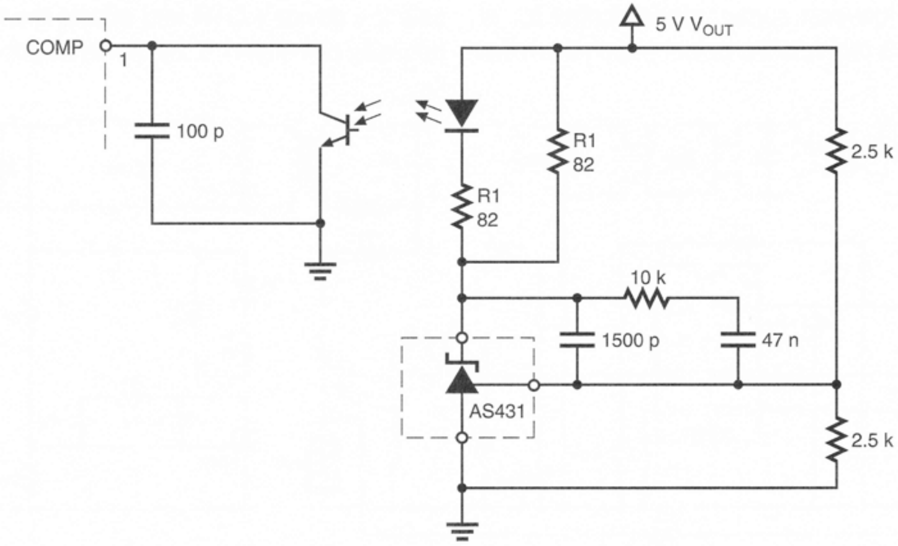


Figure 2.

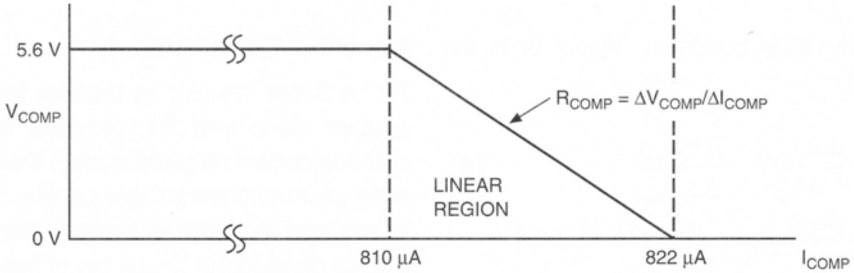
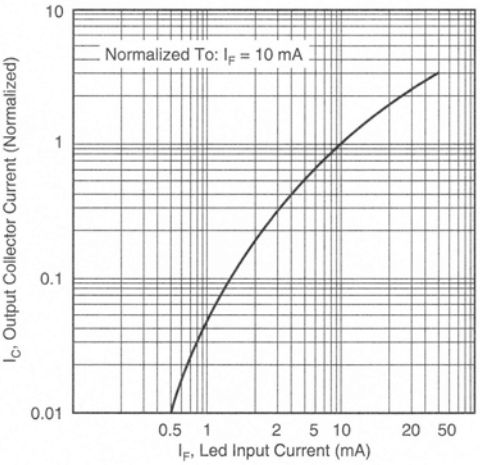


Figure 3. V_{COMP} vs I_{COMP}

Since the I_{COMP} source current is equal to the opto-coupler output current, the opto-coupler output current also modulates in the same I_{COMP} linear region. With a known opto-coupler output current, the input diode current, I_{DIODE}, can then be obtained from the output current versus diode current curve on the opto-coupler data sheet. Figure 4 illustrates the output current versus diode current curve of the 4N27 opto-coupler. The 4N27 data sheet guarantees a minimum of 0.1 CTR at 10 mA diode current.



The typical AS3842 maximum I_{COMP} source current is 800 µA. Using Figure 4, and assuming 0.1 CTR at 10 mA diode current, the forward diode current required to generate 800 µA of opto-coupler current is 8 mA.

IVb. AC Gain Analysis

Once the opto-coupler diode current is determined, the current limiting resistor R1 of Figure 2 can then be chosen to guarantee good output regulations and proper dynamic loop response. The AS431 cathode voltage, $V_{CATHODE}$, is a function of the diode operating current, I_{DIODE}, and the value of R1. Also, $V_{CATHODE}$ must be greater than 2.5 V for proper operation.

$$\begin{aligned} V_K &= V_O - V_D - (I_D \cdot R1) > 2.5\ V \qquad (1) \\ &= 5.0\ V - 1.2\ V - (8\ mA \cdot R1) > 2.5\ V \\ &= 3.8 - (8\ mA \cdot R1) > 2.5\ V \\ R1 &< 162\ \Omega \\ &= 82\ \Omega\ (chosen) \\ V_K &= 3.14\ V \end{aligned}$$

R1 also plays asignificant role in controlling the open loop gain of the power supply. The following equations derive the small signal AC gain from $V_{CATHODE}$ to V_{COMP}.

$$\begin{aligned} I_{COMP} &= I_D \cdot CTR \qquad (2) \\ &= \frac{(V_O - V_K)}{R1} \cdot CTR \end{aligned}$$

$$\frac{\Delta I_{COMP}}{\Delta V_K} = -\frac{CTR}{R1} \qquad (3)$$

At the steady state condition, V_{COMP} is in the linear region,

$$\frac{\Delta V_{COMP}}{\Delta V_K} = \frac{\Delta I_{COMP}}{\Delta V_K} \cdot \frac{\Delta V_{COMP}}{\Delta I_{COMP}} \tag{4}$$

$$= \frac{CTR}{R1} \cdot R_{COMP}$$

From figure 3:

$$R_{COMP} = \frac{\Delta V_{COMP}}{\Delta I_{COMP}}$$

$$= \frac{5.6\ V}{(822 - 810)\ \mu A}$$

$$= 509\ k\Omega$$

Applying equation (4):

$$\frac{\Delta V_{COMP}}{\Delta V_K} = \frac{0.1}{82\ \Omega} \cdot (509\ k\Omega)$$

$$= 620$$

$$= 55.9\ dB$$

IVc. Other Considerations

R2, a 2 kW resistor in parallel with the opto-coupler diode and R1, provides the minimum cathode current required to keep the AS431 operating when a minimum opto-coupler diode current is required. In addition, a small filter capacitor is placed close to the V_{COMP} pin of the control IC to attenuate high frequency switching noise being picked up by the metal trace from the opto-coupler to the control IC. Since the location of the pole in the opto-coupler small signal response varies significantly with the dc operating point of the opto-coupler, a resistor can be added from the V_{REG} to V_{COMP} pin to supply additional bias current to stabilize the loop.

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ASTEC

AS1200

Application Note 3

Power Good and Over-voltage Sensing Using the AS1200

Mike Wong

I. Introduction

Recently, the power good function has gained tremendous popularity in PC power supply designs because it can initiate a start-up procedure for the microprocessor after the power supply's outputs reach their regulation ranges. It can also warn the microprocessor before a power failure occurs. This paper gives a practical design example of housekeeping functions in a two FET forward switching power supply. The housekeeping scheme described in this paper is implemented with the AS1200, an advance general purpose housekeeping IC designed for under voltage and over-voltage detection and AC input voltage sensing.

II. Specifications

The application shown is designed to meet the following specifications:

Over-voltage:

+5 V output: +6 ± 0.5 V
+12 V output: +13 ± 0.5 V
–12 V output: –13 ± 0.5 V

Under-Voltage:

+5 V output: +4 ± 0.5 V
+12 V output: +11 ± 0.5 V
–12 V output: –11 ± 0.5 V

V_{AC} input ($_{\text{TURN-ON}}$): 78 V_{AC}

V_{AC} input ($_{\text{TURN-OFF}}$): 66 V_{AC}

POK signal delay time after all rails reach their OK values: 350 ms

POK output Characteristics:

TTL Signal (Low state): Less than 0.4 V with 5 mA sink current

TTL Signal (High state): Greater than 2.5 V with 1 mA source current

III. Complete Schematic

Figure 1 shows the complete schematic of a power supply with the housekeeping functions. All components mentioned in this report are shown in this schematic. Only the housekeeping functions are discussed extensively. Many of the calculated components have non-standard values. The chosen standard component values are included in parentheses.

IV. Over-voltage Detection

An over-voltage sensing network can be simply implemented with voltage dividers. The POV (pin 2, positive over-voltage) is internally referenced to 2.5 V and the NOV (pin 3, negative over-voltage) is referenced to ground. If either the POV is pulled above 2.5 V or the NOV is pulled below ground, the OVP (pin 14, over-voltage protection) output goes high to within 2 volts of V_{CC}. A high OVP output is capable of sourcing 500 mA to drive an SCR to latch off the power supply.

Positive Over-voltage

D13 provides a wired OR function of the +5 V and +12 V outputs, and the result is divided down by R40, R41, and R42 and fed into the POV pin.

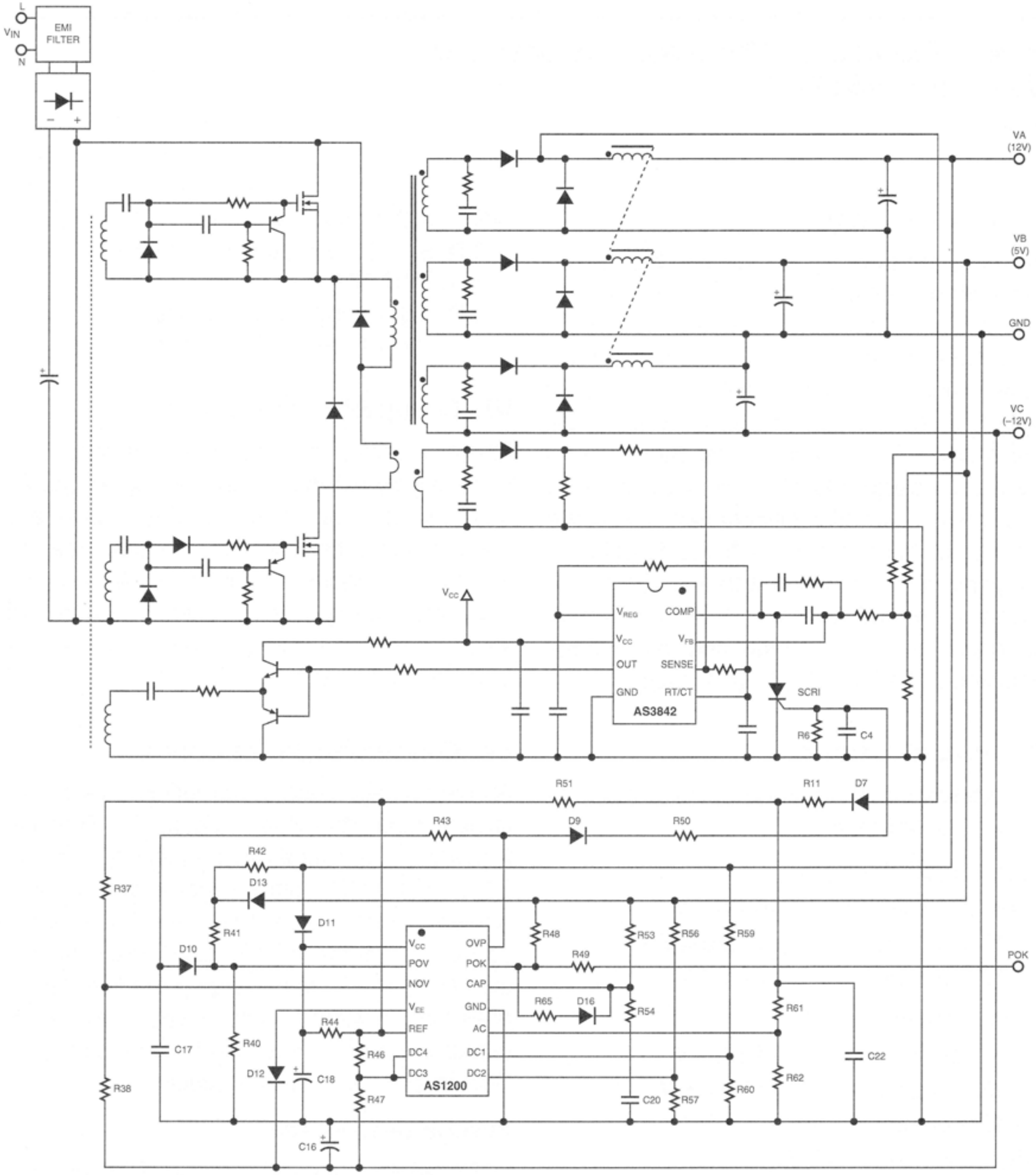

Figure 1. AS1200 Design Example

V_{REF} = internal reference of the AS1200
= 2.5 V

V_{DIODE} = diode voltage of D13
= 0.7 V

OV5 = +5 V nominal over-voltage trip point
= 6 V

OV12 = +12 V nominal over-voltage trip point
= 13 V

Assuming 1 mA flows through R40 when over-voltage occurs:

$R40 = V_{REF}/1\ \text{mA}$
$= 2.5\ \text{V}/1\ \text{mA}$
$= 2.5\ \text{k}\Omega\ (2.4\ \text{k}\Omega)$

$R41 = (OV5 - V_{DIODE} - V_{REF})/1\ \text{mA}$
$= (6 - 0.7 - 2.5)\ \text{V}/1\ \text{mA}$
$= 2.8\ \text{k}\Omega\ (2.7\ \text{k}\Omega)$

$R42 = (OV12 - OV5 + V_{DIODE})/1\ \text{mA}$
$= (13 - 6 + 0.7)\ \text{V}/1\ \text{mA}$
$= 7.7\ \text{k}\Omega\ (7.5\ \text{k}\Omega)$

Negative Over-voltage

From –12 V to V_{REF}, the over-voltage is divided by R37 and R38 and sensed by the NOV pin. Assuming 1 mA flows through R37 and R38 when negative over-voltage occurs:

$\underline{OV12}$ = –12 V nominal over-voltage trip point
= –13 V

$R37 = V_{REF}/1\ \text{mA}$
$= 2.5\ \text{V}/1\ \text{mA}$
$= 2.5\ \text{k}\Omega\ (2.4\ \text{k}\Omega)$

$R38 = |\underline{OV12}|/1\ \text{mA}$
$= 13\ \text{V}/1\ \text{mA}$
$= 13\ \text{k}\Omega$

OVP Latch

When an over-voltage condition is detected, the OVP pin goes high. R43 and D10 provide a path for the high OVP voltage to feed back to the POV pin to latch the AS1200 in the over-voltage condition.

$R43 = (V_{CC} - 2\ \text{V} - V_{REF} - V_{DIODE})/1\ \text{mA}$
$= (11.3 - 5.2)\ \text{V}/1\ \text{mA}$
$= 6.1\ \text{k}\Omega\ (6.2\ \text{k}\Omega)$

C17 sets the minimum over-voltage duration necessary for the OVP latch to be engaged. A minimum over-voltage duration prevents the OVP latch from false triggering during power supply output step load test when the output goes high for a short period of time.

Power Supply (SCR) Latch

If an over-voltage condition sustains for a certain period of time set by R50, R6, and C4, the SCR1 turns on and latches off the power supply.

V. Under-voltage Detection

Under-voltage sensing simply involves working out resistor dividers. After all outputs reach their OK levels, the POK becomes high impedance after a time delay. This POK time delay is controlled by selecting the proper timing resistor and capacitor values for the CAP pin. In this application, an under voltage condition causes the Cap pin to go low but will not latch off the power supply. Power supply under voltage latching off can be accomplished by connecting a capacitor from the CAP pin to the NOV pin.

Positive Under-voltage

DC1 and DC2 comparators are used to sense +12 V and +5 V. Assuming 1 mA going through those sensing resistors:

For +12 V, DC1 comparator is used:

UV12 = +12 V nominal under voltage trip point
= 11 V

R60 = V_{REF}/1 mA
= 2.5 V/1mA
= 2.5 kΩ (2.4 kΩ)

R59 = (UV12 – V_{REF})/1 mA
= (11 – 2.5) V/1 mA
= 8.5 kΩ (8.2 kΩ)

For +5 V, DC2 comparator is used:

UV5 = +5 V nominal under voltage trip point
= 4 V

R57 = 2.5 kΩ (2.4 kΩ)

R56 = (UV5 – V_{REF})/1 mA
= (4 – 2.5) V/1 mA
= 1.5 kΩ

Negative Under-voltage

A resistor divider for the negative under-voltage sensing can be calculated in exactly the same manner as for the positive under voltage sensing. Since this power supply has only one negative output, inputs for DC3 and DC4 comparators are connected together. Assuming 1 mA going through those sensing resistors:

For –12 V, DC3 and DC4 are used:

$\underline{UV12}$ = –12 V nominal under voltage trip point
= –11 V

R46 = V_{REF}/1 mA
= 2.5 V/1 mA
= 2.5 kΩ (2.4 kΩ)

R47 = $\underline{|UV12|}$ /1 mA
= 11 V/1 mA
= 11 kΩ

AC Sensing

The AC comparator monitors the input line voltage and trips the UV comparator if the line voltage is too low. To maintain isolation, the AC line voltage is sensed on the secondary winding. When the FET is turned on, the bulk cap voltage is stepped down by the power transformer windings and coupled to the secondary. The secondary voltage waveform is then rectified by a diode, a resistor, and a capacitor (D7, R11, and C22 in Figure 1) and divided down and fed into the AC comparator. An open collector latch at the AC comparator also allows for hysteresis design. The input line UVLO turn on and turn-off and hysteresis of the power supply can be calculated:

N = transformer turns ratio
= 3.5:1

V_{REF} = internal reference of the AS1200
= 2.5 V

V_{DIODE} = diode voltage
= 0.65 V

R_{AC} = internal AC comparator latch resistance
= 25 kΩ

$$V_{AC(\text{TURN - ON})} = \frac{N}{\sqrt{2}} \left\{ V_{REF} \left(\frac{R61\,(R_{AC} + R62)}{R62 \cdot R_{AC}} + 1 \right) + 2V_D \right\}$$

$$V_{AC(\text{TURN - OFF})} = \frac{N}{\sqrt{2}} \left\{ V_{REF} \left(\frac{R61 \cdot R62}{R62} + 1 \right) + 2V_D \right\}$$

$$V_{AC(\text{HYSTERESIS})} = V_{AC(\text{TURN - ON})} - V_{AC(\text{TURN - OFF})}$$

$$= \frac{N}{\sqrt{2}} \left(V_{REF} \frac{R61}{R_{AC}} \right)$$

$$V_{IN\,(\text{HYSTERESIS})} = V_{IN\,(\text{TURN - ON})} - V_{IN\,(\text{TURN - OFF})}$$

$$= 78 - 66\ V_{AC}$$

$$= 12\ V_{AC}$$

For a 12 V_{AC} hysteresis, solve for R61 in equation (3):

R61 = 47 kΩ

Using R61 and V_{AC} (turn-off), solve for R62 in equation (2):

R62 = 5.1 kΩ

Another important component that needs to be considered is C22. The value of C22 has to be sufficiently high such that the voltage ripple on C22 is smaller than the hysteresis set by R61.

C22 = 100 nF

A 22 Ω resistor (R11) is added in series with D7 to create a low pass filter.

POK Delay

R53, R54, and C20 determine the required time delay for the POK signal after all outputs reach their OK values. The CAP pin is an open collector output of the under voltage comparators. When all power supply outputs elevate above their under voltage levels, the CAP Pin becomes high impedance and allows C20 to be charged through R53 and R54. When the CAP voltage reaches above V_{REF}, the POK output goes high.

$$\text{POK } T_D = -\,(R53 + R54)\,(C20)\ \ln\left(1 - V_{REF}/5\text{ V}\right)$$

For a POK Delay Time of 350 ms:

C20 = 0.22 mF

R53 = 2.2 MΩ

R54 = 100 Ω

To decrease the POK comparator's long transition time and provide immunity against noise ripple on the C20 charging slope, a pull-up resistor and a diode (R65 and D16) are connected in series from the POK pin to the CAP pin. This pulls the CAP pin higher after the POK comparator is tripped. R65 and D16 can also be replaced by a small capacitor. The small resistor R54 limits the discharge current of C20 into the CAP pin and allows the CAP pin to be pulled high instantaneously.

R65 = 10 kΩ

In this example, the power supply spec for the POK output calls for a voltage greater than 2.5 V and a source current of at least 1 mA when POK goes high:

$$R48 \le (5\ \text{V} - 2.5)\ \text{V}/1\ \text{mA}$$
$$\le 2.5\ \text{k}\Omega\ (2.2\ \text{k}\Omega)$$

When POK goes low, the POK output spec calls for less then 0.4 V with 5 mA I_{SINK}:

$$R49 \le 0.4\ \text{V}/5\ \text{mA}$$
$$\le 80\ \Omega\ (56\ \Omega)$$

VI. V_{REF}, V_{CC}, and V_{EE} Biasing

V_{REF}

Because the reference is designed to be independent of the supply voltages V_{CC} and V_{EE}, the reference pin needs 4 to 8 mA of external shunt current to operate. In Figure 1, R44 connected from V_{CC} to V_{REF} supplies current to power the shunt reference circuitry.

$$\begin{aligned} R44 &= (V_{CC} - V_{DIODE} - V_{REF})/8\ \text{mA} \\ &= (12 - 0.7 - 2.5)\ \text{V}/8\ \text{mA} \\ &= 1.1\ \text{k}\Omega \end{aligned}$$

During initial start-up and before +12 V output comes up, the reference is pulled high by the AC signal through R51.

V_{CC}

V_{CC} needs 5 to 18 volts to operate. In Figure 1, a small electrolytic capacitor C18 and a reverse blocking diode D11 are placed at the V_{CC} pin to increase the hold-up time of the AS1200. Longer hold-up time allows the AS1200 to operate for a few milliseconds after a fault condition is detected.

$$C18 = 82\ \text{mF}$$

Assume the worst case discharge current of 16.5 mA:

$$\begin{aligned} t_D &= \Delta V\ (C18/I_{DISCHARGE}) \\ &= (12 - 0.7 - 5)\ \text{V}/0.2\ \text{mF}/16.5\ \text{mA} \\ &= 31\ \text{ns} \end{aligned}$$

Therefore, hold-up time can be approximated at 31 ms.

V_{EE}

To ensure proper operation of the AS1200, the range of V_{EE} needs to be –2 to –14 V. As shown in Figure 1, C16 and D12 provide the hold-up time of the negative rail.

$$C16 = 82\ \mu\text{F}$$

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ASTEC

UC/AS384x
Application Note 4

Noise and Stability Considerations Using the UC/AS384x

Mike Wong

I. Introduction

The AS384x product series is a state-of-the-art power supply controller designed with high-performance circuit techniques to improve speed and accuracy. Care is required to make effective use of this product's high speed and accuracy, because noise sensitivity is an inherent consequence of peak current mode control. This can lead to jitter at the output of the IC and periodic oscillations on the output of the power supply.

II. Peak Current Mode Control

Current mode control offers several significant advantages over voltage mode control. These include automatic input voltage feed-forward, pulse-by-pulse current limiting, and lower circuit complexity.

Current mode control uses two control loops, a current loop and a voltage loop. Figure 1 shows a simplified current mode controlled buck converter.

When the FET is turned on, current through the transformer, which is proportional to the output inductor current, is sensed with the current sense resistor (R_{SENSE} in Figure 1). When the voltage level across R_{SENSE} reaches Verror (a function of the output voltage) the FET is switched off. Figure 2 illustrates the waveforms of the current mode converter shown below.

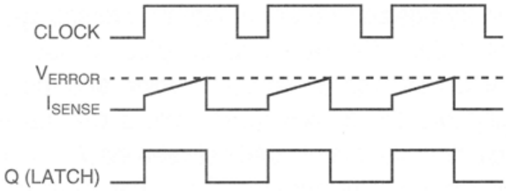


Figure 2.

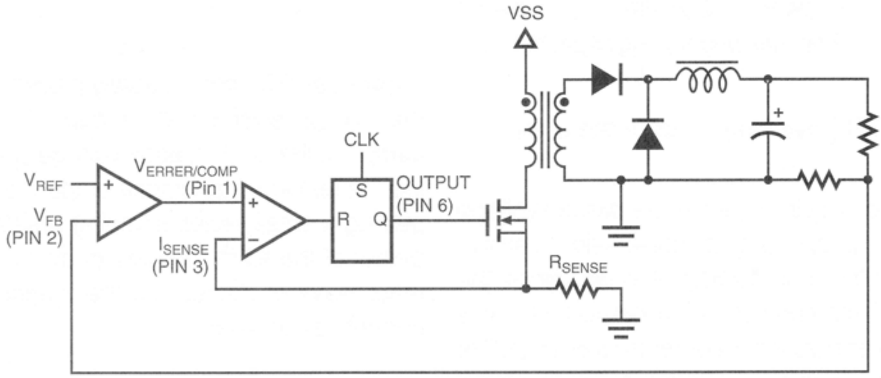


Figure 1.

III. Noise and Stability Considerations

The clock, error amplifier, current sense comparator, and RS latch are incorporated into the 384x family of IC's. Verror/Comp is the error amplifier output (pin 1). VFB is the error amplifier feedback input that senses the converter's output voltage (pin 2). I_{SENSE} is the current sense comparator input (pin 3). Below is a pin-by-pin description of how noise can be injected into the control loops and the 384x.

A. Pin 1: Verror/Comp [error amplifier output]

The Verror pin, also identified as Comp pin in the 384x, is typically used to provide feedback loop compensation for the error amplifier. If no external signal is applied to this pin and the loop compensation network is laid out close to the control IC, this pin will not experience noise problems. However, if the power supply is controlled on the primary side and the Verror signal is created by an AS431-2.5V Reference IC coupled across the isolation through an optical coupler, and fed directly into the 384x's Verror pin, a decoupling capacitor is recommended between the Verror pin and ground. The purpose of this capacitor is to filter any noise picked-up from the output of the AS431. Extreme care must be taken in selecting this decoupling capacitor because an excessively large capacitor creates an extra pole into the voltage control loop, which can lead to instability problems. In a power supply with proper lay-out and compensation, this decoupling capacitor may be avoided.

B. Pin 2: VFB [inverting input of the error amplifier]

The signal to this pin comes from a divided voltage in the power supply output. Noise seldom enters into the control loop through this pin, since the error amplifier's compensation network is a low pass filter with a very low corner frequency (1/3 of the switching frequency). This network filters out any noise on the VFB pin.

C. Pin 3: Isense [current sense input for the PWM comparator]

The signal to this pin is usually a voltage level proportional to the output inductor current. The 384x output gate drive pulse is terminated when the voltage at I_{SENSE} reaches V_{ERROR}. Most noise-related problems can be traced directly to this pin. One can generally categorize these problems into four groups: leading edge current spike on the current sense waveform, periodic oscillation or noise on the current sense waveform, peak to average current error, and instability caused by greater than 50% duty cycle.

IV. Noise Characteristics Related to Current Sense

A. Leading Edge Current Sense Spike

During the transient when the MOSFET is being switched on, an instantaneous voltage is induced across the power transformer to generate a high surge current through the power MOSFET to ground. This surge current creates a leading edge voltage spike as shown in Figure 3.

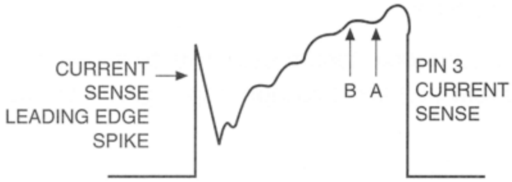


Figure 3.

A low pass RC filter is usually placed in-between the R_{SENSE} resistor and the current sense pin to damp out the leading edge voltage spike. Reducing the leakage inductance of the transformer or placing a small series damping resistor from the output of the IC to the gate of the MOSFET are other ways of decreasing the magnitude of the current sense spike.

B. Periodic Oscillation on the Current Sense Waveform

By examining the current sense signal carefully (Figure 3), a high frequency ringing can be seen superimposed on the current sense ramp. This ringing is caused from parasitic elements in the current sense loop and also from noise being coupled across the leading edge low pass filter capacitor. Because manufacturers of the 384x have different current sense comparator circuitry and wafer processes, their comparator bandwidths can be quite different. As a result, one manufacturer's 384x may be more "noise sensitive" than another. For example, in Figure 3, the 384x's output is set to turn off at point A but because of its wide bandwidth, the 384x can be false-triggered at point B. As a result, the duty cycle is reduced prematurely and results in jitter and instability problems. However, if the IC's comparator bandwidth is smaller than the frequency of the ringing oscillation, the ringing is ignored or filtered out by the IC.

If a 384x's current sense comparator bandwidth is larger than the ringing frequency, the effects of the ring can be minimized by increasing the voltage ramp of the slope compensation. (Slope compensation is discussed extensively in section V.) The purpose of increasing slope compensation is to improve the current sense signal to noise ratio, or the ratio of the magnitude of the current ramp to the magnitude of the ringing.

C. Peak vs. Average Current Error

Current mode control regulates the peak inductor current, but the converter's output current corresponds to the average inductor current. Figure 4a shows the output current (average inductor current) increases as the duty cycle increases. Consequently, the line regulation is degraded because the converter delivers different amounts of current at different line conditions (Duty Cycle = V_{OUT}/V_{IN}). Figure 4b and 4c illustrate how this problem can be corrected with slope compensation.

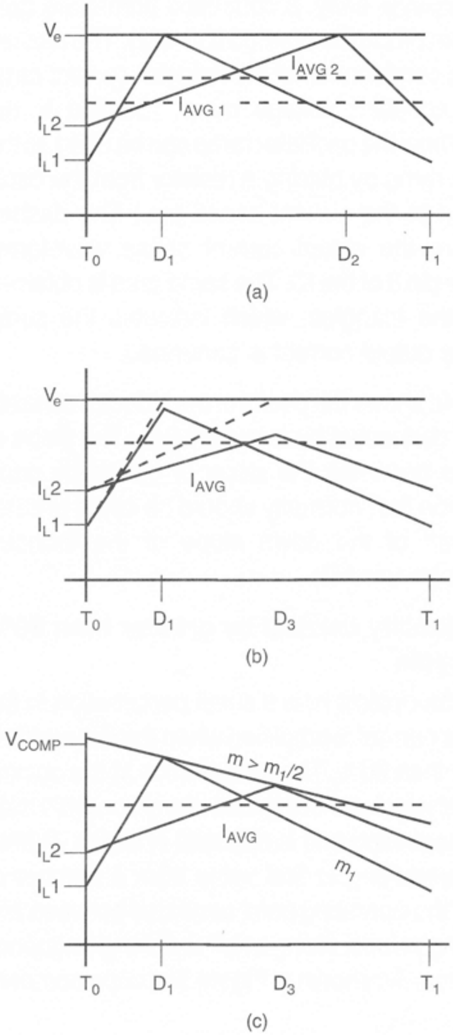


Figure 4.

Figure 4a shows the average inductor current (Iavg1 and Iavg2) in dashed lines changes as the duty ratio (D1 and D2) changes. The triangles formed by solid lines represent the actual inductor currents (IL1 and IL2) at different duty ratios (D1 and D2), and the areas under the triangles are their average currents.

Figure 4b shows that if an additional voltage ramp is introduced onto the current sense ramp to elevate the current sense ramp and allows it to reach V_{ERROR} early, a controlled premature gate drive turn off can be created (D3<D2). The dashed line is a combination of the inductor current ramp and a constant voltage ramp. (Section V describes how the oscillator ramp can be used as the voltage ramp by placing a resistor from the oscillator pin to the current sense pin.) The dashed lines are the actual current sense waveforms seen by pin 3 of the IC. The same area is obtained under the triangles, which indicates the same average output current is generated.

Figure 4c shows the peaks of the inductor currents can be connected by a straight line. The slope of this line becomes the slope of our slope compensation that normally should be set at greater than half of the down slope of the inductor current ($m \geq m1/2$).

D. Instability caused by greater than 50% duty cycle

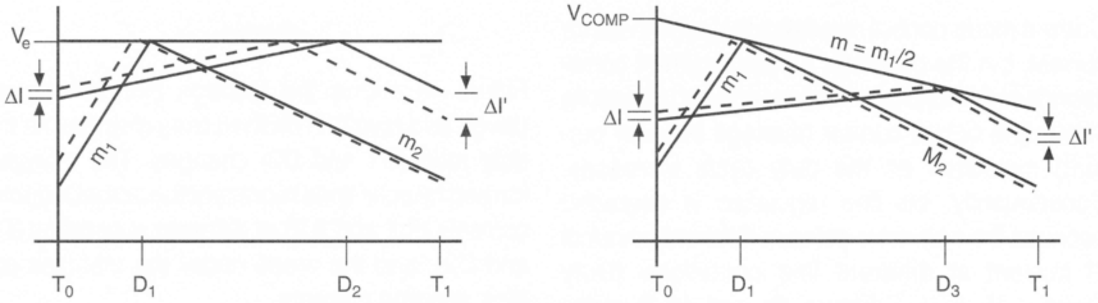
Figure 5a depicts how a small perturbation in the inductor current is amplified when the duty cycle is greater than 50%. The perturbation in the operating point is greater at the end of a given cycle than at the beginning and is opposite in sense. Rather than converging to find value after a number of cycles, the operating point oscillates between two diverging values, giving a half switching frequency oscillation. As shown in Figure 5b, slope compensation again can be used to attenuate the error caused by the perturbation.

V. Implementation of Slope Compensation

Slope compensation is usually implemented with an additional resistor, R_{SLOPE}, placed between pin 3 and pin 4 of the IC, as shown in Figure 6a. The magnitude of the slope is determined by R_{SLOPE} and R1, the resistor for the low pass filter. Generally, the slope is set at greater than half of the down slope of the inductor current ($\text{Slope} \geq m1 / 2$). A small parallel capacitor, C_{SLOPE} in Figure 6a, is suggested to enhance operation at minimum duty cycle and light loads. In some cases, the addition of R_{SLOPE} may affect the oscillator frequency and duty cycle. Another slope compensation circuit (Figure 6b) is suggested to avoid the frequency shift problem. In Figure 6b, a voltage ramp with positive slope is generated by R_{SLOPE} charging C_{SLOPE} when the output is turned on. This voltage ramp is added onto the current sense waveform through Rb, a buffer resistor. Another advantage of this slope compensation circuit is that the slope can be easily adjusted by changing R_{SLOPE} or C_{SLOPE}.

VI. AS384x

The Astec 384x is designed to provide a number of improvements over the competitor's standard UC384x. Some of the improvements are guaranteed oscillator discharge current, reduced current sense to output delay (for high frequency operations), and an exact 50% duty cycle clamp for the



(a) (b)

Figure 5.

AS3844/5. However, a couple of simple design considerations allows the improved AS384x to be used identically to the designs of other manufacturers.

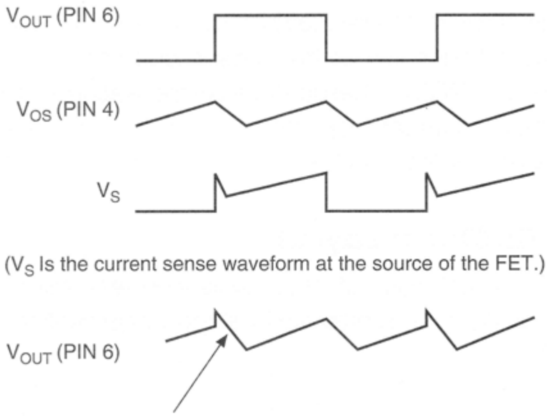
A. Slope Compensation With the AS3844/5

In order to guarantee a true 50% duty cycle output clamp, the AS3844/5 is implemented with an alternate "on" cycle scheme. The output of the IC is latched "on" at the peak of the oscillator and turned "off" when the oscillator reaches its next peak. This is illustrated in Figure 7. If the slope compensation is implemented with the scheme shown in Figure 6a (with a resistor going from the oscillator pin to the current sense input), the down slope of the oscillator can be superimposed onto the current sense waveform. This creates a false high signal that can prematurely turn off the gate drive output. Figure 7 illustrates all the associated waveforms.

One of the simplest ways to implement slope compensation and avoid the current sense false trigger problems is illustrated in Figure 6b and described in Section V.

B. Bandwidth of the AS384x

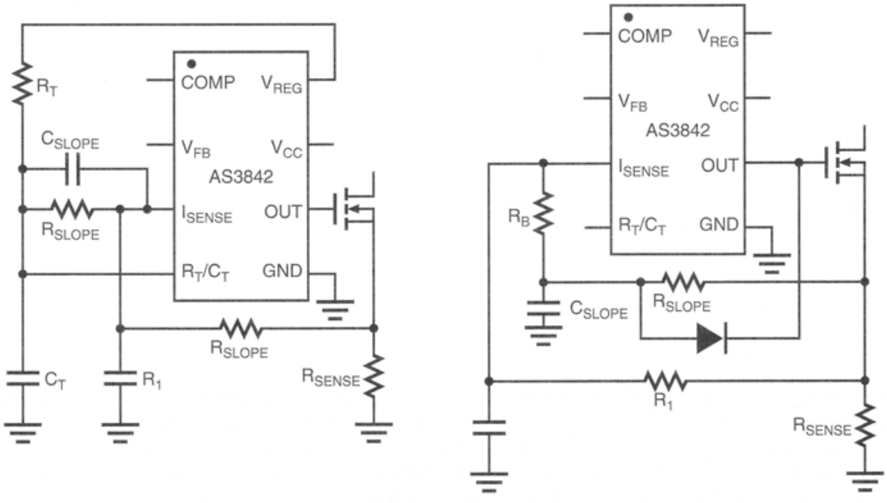
Since the AS384x is designed for high switching frequency operations, the current sense to output



(V_S Is the current sense waveform at the source of the FET.)

This is the result of superimposing V_{OS} on V_S. This leading edge voltage spike could falsely trigger the current sense comparator and cause noise problems.

Figure 7.



(a) (b)

Figure 6.

delay time is reduced and the bandwidth of the current sense comparator increased to ensure the converter senses and responds to signals at switching frequencies above 500KHz. As explained previously in section IVB, an IC with a wide current sense comparator bandwidth is more susceptible to noise. If a fast current loop is not required in the application, the frequency response (or the cross over frequency) of the current loop can be reduced. With increased slope compensation and a slower current loop, the AS384x functions the same as other 384x's.

VII. Circuit Layout

Incorrect layout can cause severe noise problems that cannot be corrected by slope compensations or decoupling. The following is a list of some common layout rules that will help to ensure a noise-free environment for proper operation of the control circuit.

1) Keep all trace and lead lengths to a minimum.
2) Separate the power ground and signal ground.
3) Use ground planes.
4) Keep decoupling capacitors close to the IC.
5) Locate IC and control circuits away from the power devices.
6) Avoid large loops.

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AS1012
Application Note 5

500 kHz/100 W DC-DC CONVERTER

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1.0 Introduction

The purpose of this application note is to demonstrate the performance capabilities of the new ASTEC AS1012 High Frequency PWM Controller IC by describing a state of the art high performance forward DC to DC converter which was specifically developed around the AS1012.

This application note was prepared for power supply designers who have had some experience with switching power supplies and in particular with the forward converter topology.

2.0 Background

2.1 The AS1012 Integrated Circuit

The AS1012 IC is an advanced, full featured general purpose pulse width modulator (PWM) controller, intended for use in single ended high frequency switching power supplies. The 20 pin IC can be used to provide either the new current mode control or the traditional voltage mode control schemes. Although usable over a wide range of frequencies, the device was specifically designed for 500 kHz applications.

2.2 AS1012 Features

The key features of the AS1012 are listed below.

- 2.5 V_{DC} Band Gap Reference
- Uncommitted 5 MHz Op Amp
- Feedforward Control of High Frequency Oscillator
- PWM Comparator
- Uncommitted Current Limit Comparator
- Adjustable Level Under-voltage Lockout (UVLO)
- High Current Totem Pole Output
- Soft-Start
- Remote On/Off Control
- External Frequency Synchronization
- Overtemperature Shut-down
- Well Behaved High Frequency Logic
- Power and Analog Ground Pins

The functions and specifications of the AS1012 High Frequency PWM Controller IC are described in detail in the AS1012 Data Sheet.

2.3 AS1012 Applications

The AS1012 Controller may be applied to many power conversion applications, with various topologies, including resonant converters. Considering the array of features provided in one package, the IC is particularly suited to high power density supplies and converters. For example, in this application note, a 20 watts per cubic inch, 325 to 5 V_{DC}, 100 watt forward converter is described. By using the AS1012, many diverse supplies can be design including those with multiple outputs, or with high voltage, or high current, or low power consumption, to name just a few.

3.0 Example DC to DC Converter

3.1 Converter Description

The 100 watt forward converter described in this application note produces 5 V_{DC} at 20 Amps from a DC input ranging in value from 180 to 370 V_{DC}, derived off-line from 240 V_{AC} or from a doubler connected to 120 V_{AC} mains.

The prototype converter, when constructed with surface mount devices, occupies a volume of less than 10 cubic inches and weighs only 10 ounces.

Performance specifications are as follows:

• Output Voltage Range	4.95 to 5.05 V_{DC}
• Current Range	0 to 20 A
• Load Regulation	0.4% max
• Line Regulation	0.4% max
• Output Ripple	50 mVp-p max to 20 MHz
• Overcurrent Limit	21.5 A min to 23.5 A max
• Voltage Trim Range	10% min
• Efficiency	78% min
• Transient Response	200 mV peak, Setting to 10% of final value in 100 µs for a step change from 20 to 10 amps at a slew rate of 0.5 A/µs
• Operating Temperature	0 to 70°C
• Over Temperature Limit	70°C min
• Paralleled Operation	Multiple unit current sharing

3.2 Block Diagram

The block diagram of Figure 1 shows the major elements of the example 100 watt, high-performance DC to DC converter designed around the Astec AS1012 controller.

The block diagram shows all the major sections of the converter organized around the two control loops; the outer voltage control loop from the output back to the modulator and the inner current loop from the current transformer on the power stage back to the modulator, with the AS1012 integrated circuit at the core of both loops.

Employing the two-transistor forward converter topology, the converter's pulse width modulator operates at 500 kHz, and incorporates current mode control. An optical coupler provides isolated voltage feedback from the secondary side of the power transformer to the pulse width modulator (PWM) on the primary side.

Primary current in the power stage is sensed by a current transformer and fed to the AS1012 to provide pulse-to-pulse current control.

Additionally, the converter has been designed to include features such as under-voltage lockout and remote on-off capability.

3.2.1 PWM IC controller

The AS1012 High Frequency PWM Controller is described in detail in the AS1012 Data Sheet. Refer to the circuit Description Section Of the data sheet for design details.

3.2.2 Gate drive

The output of the AS1012 is fed to the single transistor buffer which drives a gate drive transformer with two identical secondaries, one for each of the two power stage transistors. Each secondary drives a gate drive circuit which includes an active pull down transistor. The transistor buffer and active pulldown transistors are

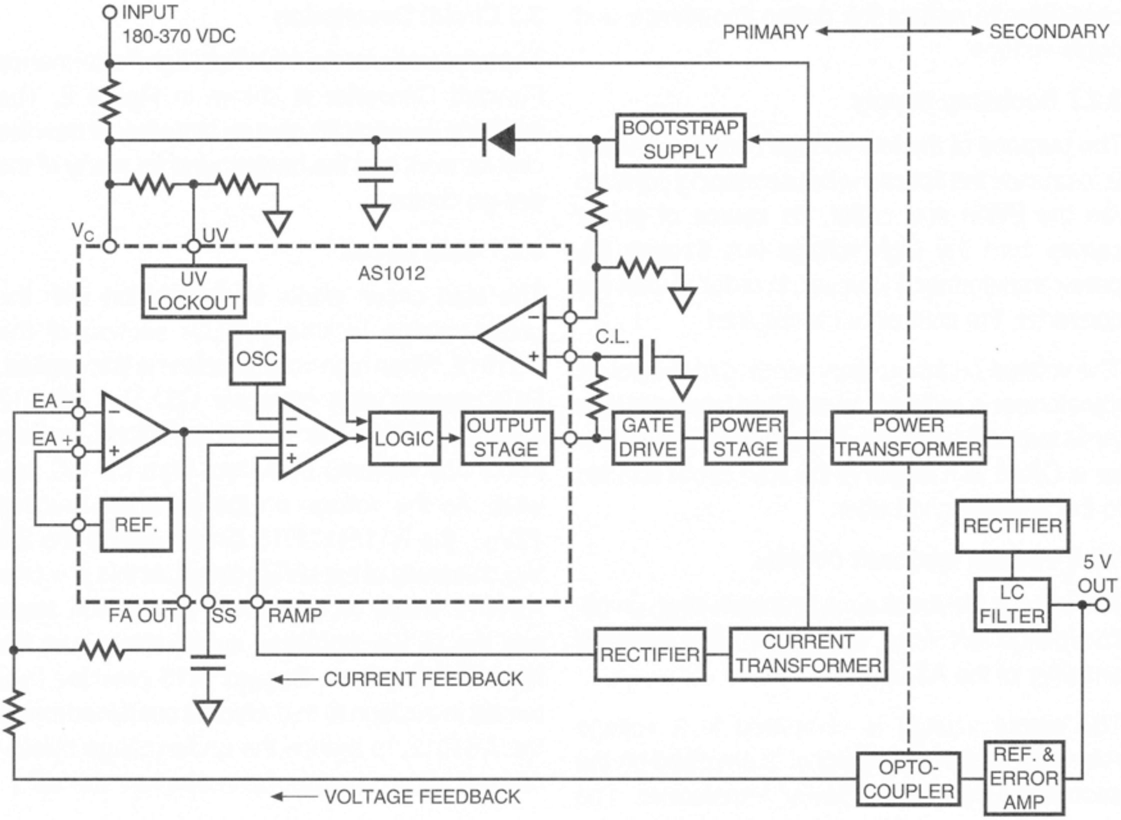


Figure 1. Block Diagram

necessary in this 500 kHz application to provide fast, efficient switching of the two power MOSFETs.

3.2.3 Power stage

The two-transistor forward converter topology was chosen for this application because it produces less voltage stress on the transistors and transformer primary than does the single transistor forward converter (370 V maximum in this application). The power stage consists of two power MOSFETs and two fast recovery diodes connected to the primary of the power transformer.

3.2.4 Power transformer

The power transformer consists of a single primary and two secondaries, one for the 5 V_{DC} output and the second for the boot-strap power supply.

3.2.5 Output rectifiers

The output rectifiers complete the topology of the forward converter. One diode conducts on the power stroke of the cycle and the other diode recirculates the inductor current in the off stroke. The rectifiers are a pair of Schottky barrier diodes chosen for high speed and low voltage drop. The pair is packaged in a single, common cathode device. To suppress high frequency noise, each diode is paralleled by a snubber consisting of 10 ohm resistor in series with a 1 nF capacitor.

3.2.6 Output filter

The filter consists of a single section inductor-capacitor network. A single, high frequency inductor is employed with a number of paralleled capacitors to reduce the output impedance and ripple voltage.

3.2.7 Bootstrap supply

The purpose of the low-voltage bootstrap supply is to provide the operating housekeeping power to run the PWM and buffer. Its source of power comes from the high voltage bus through the power transformer. However, in order to start the converter, the start circuit is required.

The voltage on an auxiliary winding of the power transformer is rectified, filtered and regulated by a three terminal regulator. The output of the regulator is ORed with output of the start circuit and fed to the AS1012 and buffer.

3.2.8 Voltage feedback circuits

The voltage feedback circuit consists of an amplifier/voltage reference, optocoupler and the error amplifier of the AS1012.

The output voltage is compared to a voltage reference and the error signal is amplified on the secondary side of the power transformer. The output of the amplifier drives the optocoupler which then supplies feedback to the error amplifier of the AS1012. The loop stability compensation network is located around the amplifier on the secondary.

3.2.9 Current feedback circuits

The current feedback circuit consists of a current transformer at the power stage and the PWM Comparator of the AS1012. The current transformer senses primary current in the power stage. The output signal from the current transformer is filtered to reduce a leading edge spike and rectified to extract the power stroke current. This signal is then fed to the Ramp input pin of the AS1012 where it is compared against the output of the error amplifier to produce pulse-to-pulse current control at the 500 kHz rate.

3.3 Circuit Description

The schematic for the 100 Watt High Performance Forward Converter is shown in Figure 2. The following paragraphs give an overview of how the circuits work and the background for many of the design choices.

3.3.1 Start circuit

The start circuit works in conjunction with the under-voltage lockout (UVLO) section of the AS1012. When high voltage power is first applied, R10 charges start capacitor C3. The AS1012 turns on but is in the "shut down" mode drawing about one milliamp of current from the RC network. As the voltage on the capacitor reaches $19V_{DC}$, the R11/R12/R13 divider attains the 2.6 V_{DC} threshold of the UVLO circuit. At this point the AS1012 snaps on, the power supply soft starts and the 15 V_{DC} bootstrap supply takes over the housekeeping load. Resistor R13 provides hysteresis in addition to that which is contained inside the AS1012, to reduce the undervoltage threshold, once the converter operation has started .

The start capacitor discharges during the startup transition and is thereafter clamped to 15 V_{DC} by the normal operating load of the AS1012 and the output of the bootstrap regulator, U3. Since the value of current in R10 is small, power dissipation is held to less than a 1/2 watt under nominal line conditions. The three terminal regulator (U3) regulates the raw bootstrap supply and prevents the start circuit from overstressing the AS1012 at the V_{CC} terminal.

3.3.2 PWM IC controller

Please refer to the AS1012 Data Sheet. Using to these two documents, the reader should be able to track the reasoning behind the following circuit considerations.

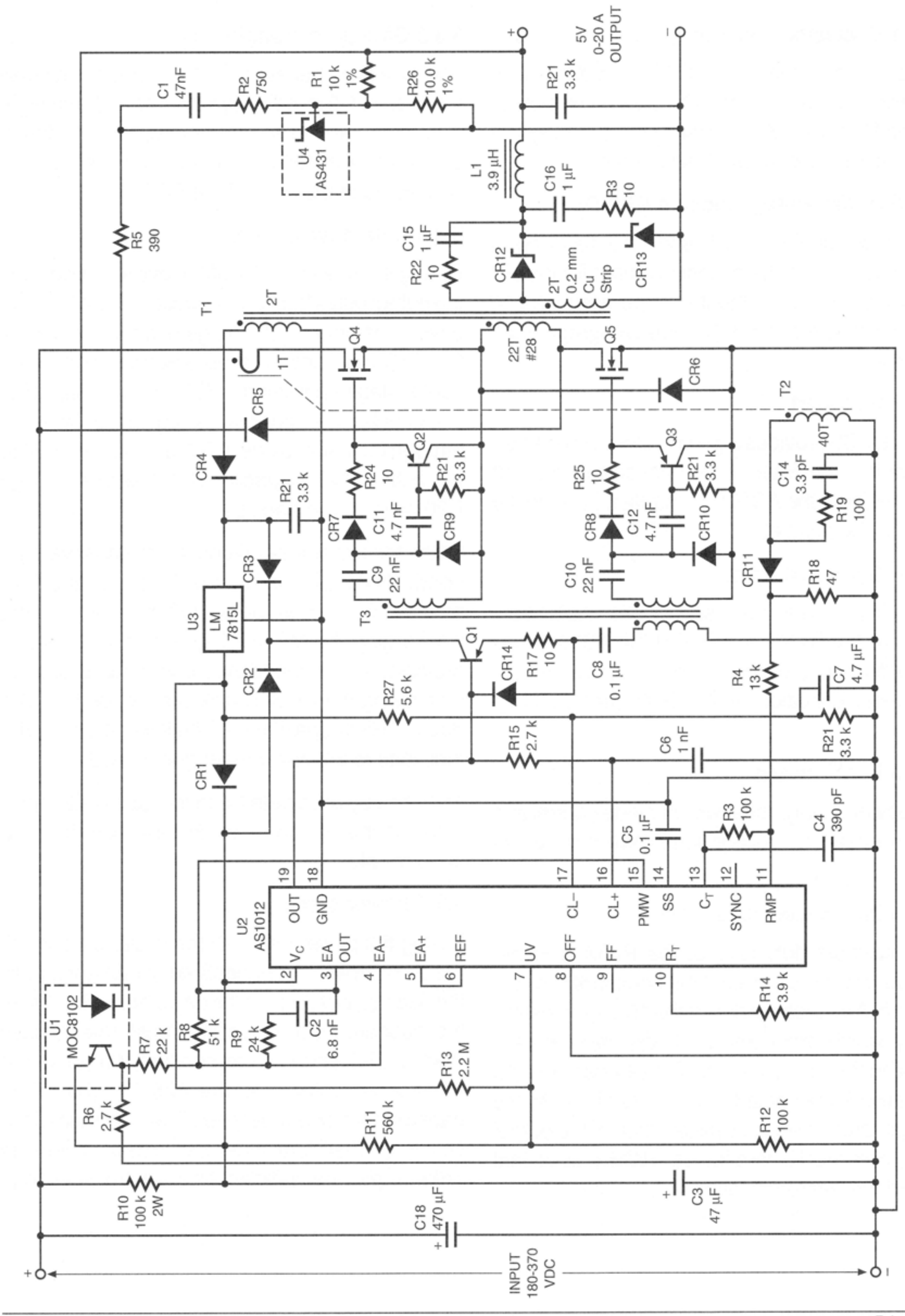


Figure 2. Schematic Diagram

3.3.2.1 Oscillator frequency

To obtain the desired switching frequency of 500 kHz, R14 was chosen to be 3.9 k ohms thereby causing C4 to be 390 pF, based on the nomograph of Figure 2.1 in the AS1012 Data Sheet.

3.3.2.2 Under-voltage lockout (UVLO)

The values of R11, R12, and R13 have been chosen to provide the necessary input for the UV pin of the AS1012 without unnecessary loading of the starting resistor, R10. See paragraph 3.3.1 for details.

3.3.2.3 Soft start

Capacitor C5 provides a gentle turn-on characteristic for the converter in accordance with the soft start feature of the AS1012 controller. Refer to the AS1012 Data Sheet.

3.3.2.4 Synchronization

Synchronization is not used in this application, therefore the SYNC terminal of the AS1012 has been left open to enable the oscillator to free run. Its default condition is the high (free-running) state.

3.3.2.5 Feedforward

This power supply uses current mode control and thus the need for voltage feedforward is not required.

3.3.2.6 Duty cycle clamp limit

The maximum duty ratio of the PWM is implemented using the current limit comparator of the AS1012. A voltage divider off the 15 V_{DC} bootstrap supply which produces a 7.5 V_{DC} level is connected to the CL – pin of the IC as a reference. An RC network connected from the OUT pin to the CL + pin produces an average value of the output pulse, and the IC terminates PWM pulses that exceed the reference value.

3.3.3 Gate drive transformer

The gate drive transformer, T3, is wound on small ferrite toroid, 9 mm OD by 5 mm ID by 3 mm high. It is trifilar wound for close coupling (24 turns, 3 × #28), with teflon insulation on the winding connected to the upper MOSFET.

3.3.4 Gate drive circuits

During the power stroke of the cycle, Q1 delivers the output pulse from the controller, U1, to the gate drive transformer, T3. The gate drive networks of C9, C10, etc., function simultaneously to drive the power stage consisting of Q4 and Q5. Capacitor C9 couples the positive going pulse from T3 through the upper diode, CR7, and resistor R24 to the gate of Q4. Capacitor C11 charges through R20, while Q2 is back biased.

When the transformer produces its negative transition, diode CR7 is reversed biased, and C11 provides base drive for Q2. Q2 thereby turns on, discharging the MOSFET gate capacitance and providing a low impedance from gate to source, minimizing the dV/dt coupling effect on the gate due to Miller capacitance. The lower diode, CR9, functions to provide a reset path for C9.

The circuitry associated with the gate of Q5 operates in identical fashion and in unison with the gate drive of Q4.

3.3.5 Power stage

During the power stroke of the cycle, Q4 and Q5 are both turned on, connecting the primary across the 325 V_{DC} bus. During the off portion of the cycle, the magnetizing current of the transformer causes diodes CR5 and CR6 to conduct, clamping the transformer voltage to the 325 V_{DC} bus. The transformer flux is thus reset. The duty ratio of the converter therefore must be limited to 50% in order to provide sufficient time for flux resetting.

3.3.6 Power transformer

The power transformer is wound on a power ferrite core with 22 turns on the primary and 2 turns on the secondaries. The core, which is 0.625 inches high, 0.75 inches wide and 1.1 inches long is a TDK PQ2016 H7C4. The primary and bootstrap windings are wound with AWG#30 while the 20 amp output secondary is wound with 0.2 mm thick copper foil with a winding resistance of 3.1 milliohms. Secondary copper loss is estimated to be 2.5 watts at 20 amps, and core loss at 500 kHz is approximately 1.4 watts at nominal line.

3.3.7 Output LC filter

The output filter inductor, L1, is a 3.9 μH, 20 A inductor wound on a PQ2016 H7C4 power ferrite core using two AWG #17 wires bifilar. The core was gapped to approximately 0.6 mm to carry the 23.5 A maximum current without saturating.

The output capacitor, C17, is actually an array of low ESR aluminum electrolytic and ceramic capacitors, to filter the voltage ripple at the output.

3.3.8 Voltage feedback circuits

The AS431 precision voltage reference and error amplifier provides secondary-side regulation of the output voltage. The output of the AS431 drives optocoupler U1, which crosses the isolation barrier and drives the AS1012 controller, U2. The error amplifier inside the AS1012 is used as an inverter, to drive the PWM input of the ramp comparator. Section 4 contains an in-depth discussion of the feedback loop operation.

3.3.9 Current feedback circuits

Current transformer T2 senses the primary current and produces a voltage across R18 which is a replica of the primary current. This signal is then combined with a compensating ramp by resistors R3 and R4, and applied to the RAMP input of the controller U2. See Section 4 for details of the current feedback operation.

4.0 Control Loop Details

Dual-loop feedback is employed in this converter to provide fast transient response and good phase margin over the full range of operating conditions. To help the designer with other applications of the AS1012, the design of the feedback circuit is described in detail herein.

4.1 Control Scheme

Figure 3 is a partial schematic diagram highlighting the control circuit. Voltage regulation is accomplished by the voltage feedback loop comprised of reference/amplifier U4, optocoupler U1, and the internal error amplifier of the IC controller U2. The current feedback loop (current-mode control) consists of current transformer T2, its terminating resistor R18, and the voltage divider of R3 and R4. The outputs of both feedback circuits are applied to the input of the comparator in U2, which determines the pulse width of the converter.

Figure 4 illustrates the control scheme in block diagram form. The system is defined in accordance with the method described in the Design Applications Manual by Analytic Artistry of Torrance, CA. Note that the modulator transfer function, K_{mod}, describes the relationship between the error voltage, V_e, and the duty ratio, d. $G_v(s)$ is the transfer function of the power stage to output voltage and $G_i(s)$ is the transfer function of the power stage to output inductor current. K_v is the transfer function of the voltage feedback amplifier. The current feedback loop is completed by the cascaded combination of K_T (the power transformer), K_i (the current transformer and its terminating resistor), and K_d (the divider ratio of R3 and R4).

The total feedback of the system is the vector sum of both the voltage and current loops. The general approach to current-mode control is to have the current loop determine the phase shift at the unity-gain crossover frequency of the system, since the current transfer function has a maximum phase lag of 90 degrees. The voltage feedback loop will have phase lag between 90 and 180 degrees, due to the LC output filter and ESR of the output capacitor. If the gain of the current loop is higher than the gain of the voltage loop, the phase shift of the current loop dominates, since the overall loop gain and phase are the vector sum of both loops. Thus, the lower phase lag of the current loop at the unity-gain crossover frequency allows stable operation without the need for phase boost in the voltage feedback loop.

A further advantage of current-mode control is the excellent input-to-output transfer function. The current feedback loop maintains constant current in the output inductor, and it does so with wide bandwidth. Thus, as the input voltage changes abruptly, the current loop quickly changes the duty ratio to compensate. Converters with current-mode control have inherently better input transient rejection than those with only voltage feedback.

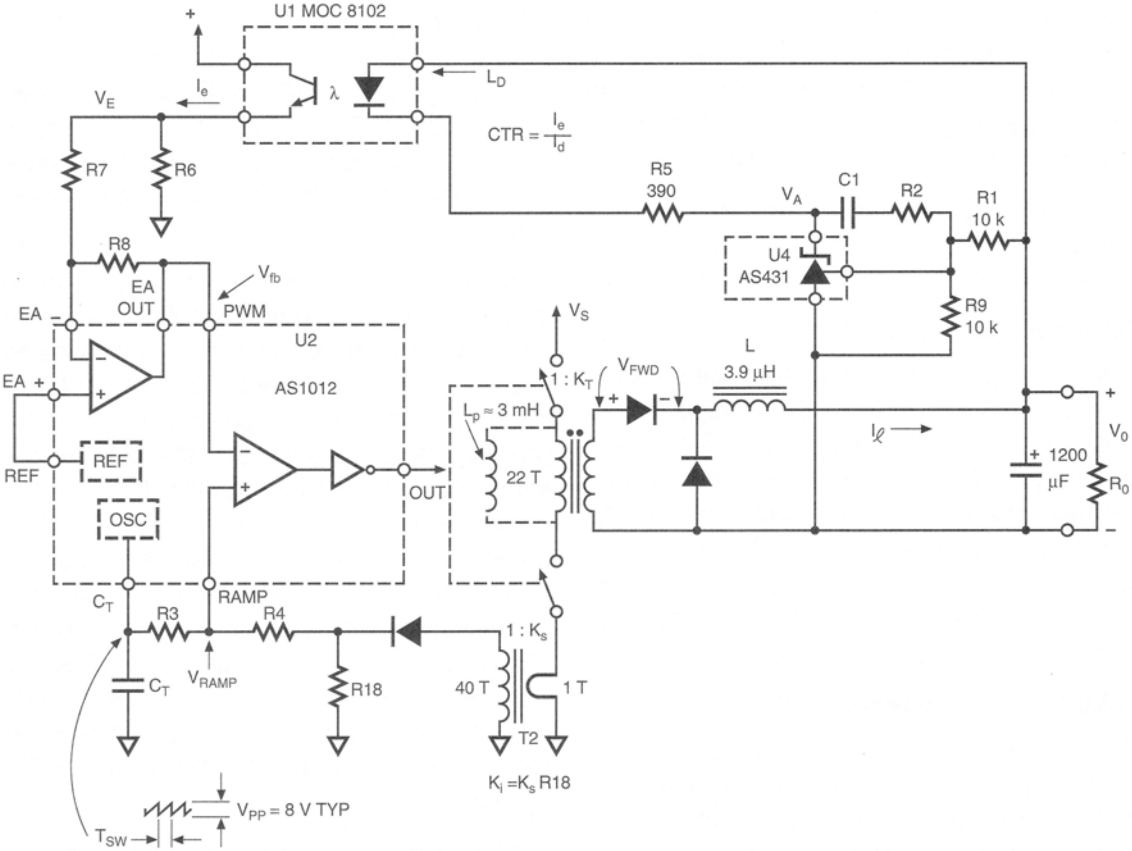
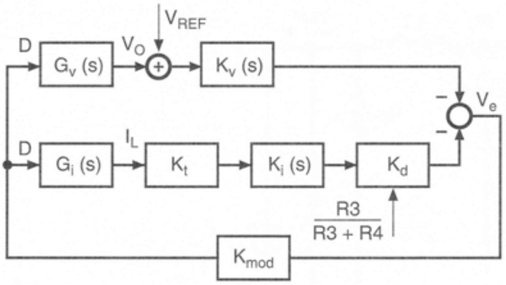


Figure 3. Control Loop Details



$$G_{OL} = K_{mod} (G_V K_V + G_i K_t K_d K_i)$$

Figure 4. Feedback Block Diagram

4.2 Design Approach

The design is done as follows:

1. Choose the unity-gain crossover frequency of the current feedback loop, usually between 1/4 and 1/10 the switching frequency of the converter.

2. Plot the gain and phase of the duty ratio-to-inductor current transfer function, $G_i(s)$ and determine the gain at the above desired crossover frequency.

3. Solve for K_d, the resistance divider ratio which attenuates the current feedback signal and introduces slope compensation from the timing ramp. This will reduce the gain of the current loop and place its unity-gain crossover at the desired frequency.

4. Solve for the necessary K_{mod}. Incidentally, K_{mod} is the reciprocal of V_{ramp}, the amplitude of the ramp at the input of the PWM comparator.

5. Plot the loop again and phase with only the current feedback to check that the loop crossover frequency agrees with the objective stated in (1) above.

6. Design the voltage feedback amplifier, with its unity-gain crossover frequency at or below the current loop crossover frequency.

7. Plot the closed loop response, to verify that the objectives are met. Also check phase and gain margins.

4.2.1 Crossover frequency

The switching frequency of this converter is 500 kHz. The crossover frequency of the current loop has been chosen at 50 kHz, which will require the voltage divider of R3 and R4 (values to be calculated in Sec. 4.2.3 below). This introduces slope compensation, which will reduce the gain of the current loop and reduce the noise susceptibility by increasing the amplitude of the ramp at the comparator.

4.2.2 $G_i(s)$

Using the capabilities of the Analytic Artistry "T_{BUCK}" software, the Bode plot of Figure 5 describes the duty ratio-to-output inductor current transfer function. Behind this Bode plot is the schematic diagram shown in Figure 6. This diagram is for the push-pull topology, but is valid for the forward converter with the circuit values shown. As shown on the plot, gain at 50 kHz is 28 dB (a factor of 25). For unity gain overall, the rest of the loop must have a gain of −28 dB, or 0.04.

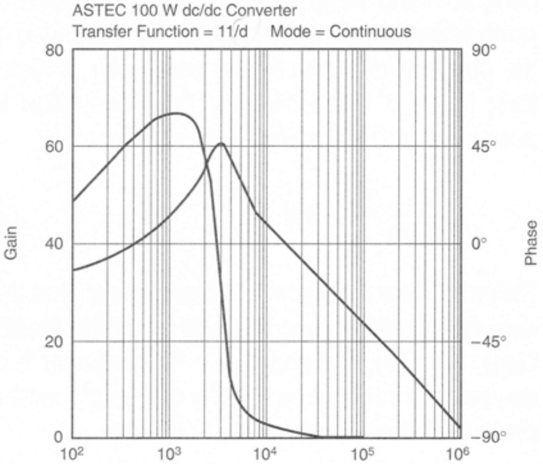
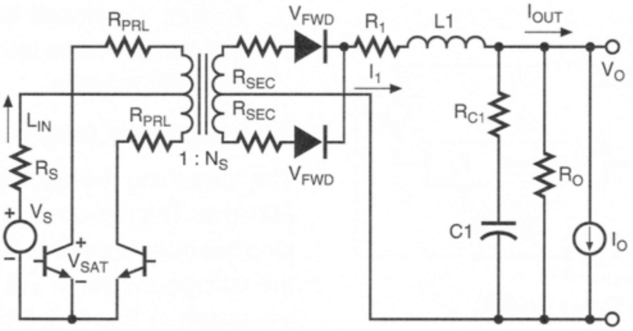


Figure 5. Duty Ratio-to-Output Inductor Current Transfer Function



R_S = .1
R_{PRL} = .1
R_{SEC} = .005
R_1 = .01
R_{C1} = .01
R_O = .5
L1 = .3.9 μH
C1 = 1200 μF
V_S = 339
V_{SAT} = 1
V_{FWD} = .5
I_O = 5
F_{SW} = 500 kHz
N_S = .091
V_O = 5

Figure 6. Schematic for Loop Analysis

4.2.3 K_d

The voltage divider ratio, K_d, describes the role of R3 and R4 in the feedback loop, as defined below:

$$Kd = \frac{R3}{R3 + R4} \tag{1}$$

As shown in Figure 3, the current feedback signal appearing at R18 is attenuated by this ratio and applied to the RAMP pin U2. Note, also, that the compensating ramp derived from the oscillator ramp which appears at the C_T pin is attenuated in the opposite direction by the same pair of resistors, R3 and R4. However, the attenuation is according to (1-K_d) rather than K_d, since:

$$\frac{R4}{R3 + R4} = 1 - Kd \tag{2}$$

Referring now to Figure 4, it can be seen that the current feed-back loop is made up of the blocks $G_i(s)$, K_t, $K_i(s)$, K_d, and K_{mod}. At crossover it is desired that this loop have unity gain, and thus the product of these factors must be unity:

$$Gi(s)KtKi(s)KdKmod = 1 \tag{3}$$

where $G_i(s)$ is taken at the desired crossover frequency and has a value of 25, as explained in 4.2.2. As shown in Figure 3, K_t is the turns ratio of the main power transformer T1, and $K_i(s)$ is the turns ratio of the current transformer T2, times the terminating resistor R18. The expression $K_i(s)$ implies that this is a frequency-dependent term (and of course it may be), but for this example it will be assumed to be frequency independent. The schematic diagram of Figure 2 shows that there is an RC filter network of R19 and C14 across the 40-turn winding of T2 filter high-frequency noise; the effect of this at 50 kHz is negligible.

K_{mod} is the modulator gain, which is $1/V_{ramp}$. V_{ramp} is shown in Figure 3 to be the RAMP input to the PWM comparator in the controller IC, U2. A signal amplitude equal to V_{ramp} applied at the PWM input of the comparator will cause the duty ratio to change from 0% to 100%, and thus the statement that $1/V_{ramp}$ is actually the modulator gain, K_{mod}:

$$Kmod = \frac{1}{Vramp} \tag{4}$$

V_{ramp} is determined by the slope of the ramp and the duration of the ramp (which is fixed and equal to the period of the oscillator). Hence,

$$Vramp = MeTsw \tag{5}$$

where T_{SW} is the period of the oscillator, as shown in Figure 3. In this case T_{SW} = 2 µs, since the frequency of the converter is 500 kHz.

M_e is the slope of the ramp, which is expressed as follows:

$$Me = KdMi + (1 - Kd)Mr \qquad (6)$$

where M_R is the slope of the oscillator ramp, or V_{pp}/T_{SW} as shown in Figure 3.

$$Mr = \frac{Vpp}{Tsw} \qquad (7)$$

M_i is the slope of the ramp appearing across R18, which is made up of two components:

$$Mi = Mi1 + Mi2 \qquad (8)$$

where M_i is the current ramp due to the primary inductance of the power transformer T1, and M_i2 is the current ramp due to the output inductor. Both of these must be calculated carefully to include the turns ratios of the power transformer and current tramsformer as necessary. As can be seen in Figure 3,

$$Mi1 = Ki\frac{Vs}{Lp} = KsR18\frac{Vs}{Lp} \qquad (9)$$

and

$$Mi2 = Ki\frac{Kt(KtVs - Vo - Vfwd)}{L} \qquad (10)$$

where L_p and L are the primary inductance of T1 and the output inductor, respectively.

Recall equation (3):

$$Gi(s)KtKi(s)KdKmod = 1 \qquad (3)$$

Equations 4, 5, and 6 can be substituted into Equation 3 to yield an equation in which the only unknown quantity is K_d:

$$GiKtKsR18Kd\,\frac{1}{Tsw(Mr\,(1 - Kd) + KdMi)} \qquad (11)$$

Rearranging this equation gives an expression for K_d:

$$Kd = \frac{MrTsw}{GiKtKsR18 + Tsw(Mr - Mi)} \qquad (12)$$

Note that the ramp slope terms M_r and M_i have not been replaced by their equivalent expressions derived in Equations 6 through 10. The reason for this is to provide a better visualization of the ramp contributors. By first calculating the value of each of the three slopes (M_r, M_i1, and M_i2), one can see how the output inductor current combines with the primary inductance and slope compensation to comprise the ramp at the PWM comparator of the control IC.

The values of M_r, M_i1, M_i2, and M_i are:

$$Mr = \frac{Vpp}{Tsw}\,\frac{8\ V}{2\ \mu s} = 4 \times 10^6 \qquad (13)$$

$$\begin{aligned} Mi1 &= KsR18\frac{Vs}{Lp} = \frac{1}{40}(47)\frac{339}{3 \times 10^{-3}} \qquad (14) \\ &= 0.132 \times 10^6 \end{aligned}$$

$$\begin{aligned} Mi2 &= \frac{1}{40}(47)\frac{0.091(0.091)\ (0.339 - 5 - 0.5)}{3.9 \times 10^{-6}} \qquad (15) \\ &= 0.69 \times 10^6 \end{aligned}$$

$$\begin{aligned} Mi &= Mi1 + Mi2 \qquad (16) \\ &= (0.69 + 0.132) \times 10^6 \\ &= 0.822 \times 10^6 \end{aligned}$$

K_d can now be determined by substituting values into Equation 12:

$$Kd = \frac{(4 \times 10^{6})(2 \times 10^{-6})}{(0.057)(47 + 2 \times 10^{-6})(4 \times 10^{6} - 0.822 \times 10^{6})} \qquad (17)$$

$$Kd = 0.886 \qquad (18)$$

4.2.4 K_{mod}

Now that K_d is known, it is a simple task to solve for V_{ramp} and its reciprocal, K_{mod}. Recall Equations 4, 5, and 6:

$$Kmod = \frac{1}{Vramp} \tag{4}$$

$$Vramp = MeTsw \tag{5}$$

$$Me = KdMi + (1 - Kd)Mr \tag{6}$$

Solving Equation 6 yields the equivalent slope, M_e:

$$Me = 0.886(0.822 \times 10^{6}) + (1 - 0.886)\,(4 \times 10^{6}) \tag{19}$$

$$Me = 1.184 \times 10^{6} \tag{20}$$

V_{ramp} and K_{mod} are then calculated as follows:

$$\begin{aligned} Vramp &= MeTsw \\ &= (1.184 \times 10^{6})\,(2 \times 10^{-6}) = 2.368 \end{aligned} \tag{21}$$

and

$$Kmod = \frac{1}{Vramp} = \frac{1}{2.368} = 0.422 \tag{22}$$

4.2.5 Checking the current feedback loop

The Bode plot of the feedback loop with only the current feedback in place is shown in Figure 7. Note that the objective of unity-gain crossover at 50 kHz has been achieved, and that the corresponding phase lag is 90 degrees, as expected.

4.2.6 Designing the voltage feedback loop

Referring to the schematic diagram of Figure 3, it is seen that the voltage loop contains three cascaded elements, namely the reference amplifier U4, optocoupler U1, and the error amplifier inside the controller U2.

Several comments are in order before proceeding:

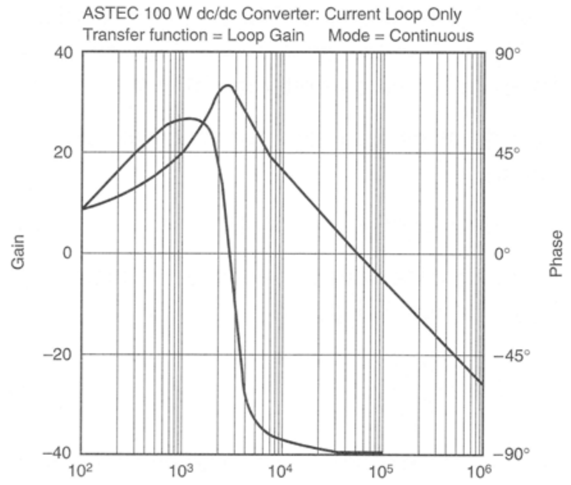


Figure 7. Loop Response with Only Current Feedback

1. Optocoupler feedback has been used for many years, and with varying degrees of success. Its simplicity and low cost are hard to beat, but the production variation of the current transfer ratio has usually caused production problems in loop stability. Now, with current-mode control, the loop stability can be made to tolerate the variations in the optocoupler, and this is further aided by the recent availability of optocouplers with tightly controlled parameters, such as the one used herein.
2. Placing the controller U2 on the primary side of the converter eliminates the need for an isolated auxiliary power supply to run the control circuitry. The AS431 reference amplifier further simplifies the system, providing both the precision reference and error amplifier in one low-cost, three-terminal device. The AS431 is pin compatible with the industry standard TL431, but is available in tighter voltage tolerance and with tighter temperature coefficient, thus eliminating the need for trimming in most cases.
3. There is a rather subtle but very important aspect of this secondary reference/amplifier

circuit which is often overlooked. It may account for some of the past difficulties in loop stability with this circuit approach. It arises from the fact that the optocoupler diode is not returned to a fixed bias voltage, but rather is connected to the voltage that is being sensed, namely V_O. The effect of this is that the feedback gain cannot be reduced to zero at high frequency, even if an infinite feedback capacitor were placed around the amplifier in the AS431. Referring to the schematic of Figure 3, it is clear that even if the output (cathode) of U4 doesn't move, perturbations on V_O are fed directly to the optocoupler via resistor R5. This is no problem, however, because there is a conventional amplifier available in controller U2 whose response can be shaped to give the required loop response.

4. It might seem that one could simply make the gain at U4 fixed (independent of frequency) at some convenient value, perhaps 10 or so, and then do all of the frequency shaping at the error amplifier in the controller U2. But the drift and component variations in the optocoupler and its associated circuitry would then translate directly back to the reference and degrade the system performance. Best performance is obtained by placing high DC gain as close to the reference as possible, namely right at U4. With this approach, the accuracy and drift are influenced only by the reference in the AS431 and the voltage divider which feeds its input from V_O.

4.2.6.1 Crossover frequency

As stated earlier, the unity-gain crossover frequency of the voltage feedback loop should be placed at or below the crossover frequency of the current feedback loop, so that the phase shift will be primarily determined by the current loop. With the current loop crossover frequency of 50 kHz, a reasonable choice for the voltage-loop crossover is an octave below, or 25 kHz.

4.2.6.2 $G_V(s)$

Figure 8 shows the Bode plot of the duty ratio-to-output voltage transfer function. As shown on the plot, the gain at 25 kHz is –6 dB, or 0.5.

$$Gv(25\ \text{kHz}) = 0.5 \tag{23}$$

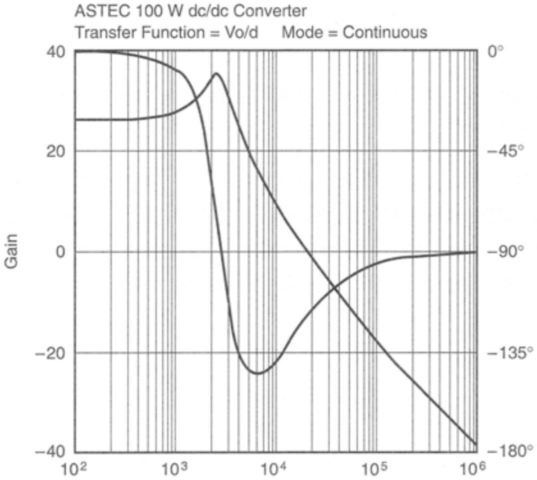


Figure 8. Duty Ratio-to-Output Voltage Transfer Function

4.2.6.3 K_V (25 kHz)

For unity gain overall, the rest of the loop must therefore have a gain of 6 dB (a factor of 2). From inspection of Figure 4, the voltage loop is described by:

$$Gv(25\ \text{kHz})Kv(25\ \text{kHz})\ Kmod = 1 \tag{24}$$

and for unity loop gain at 25 kHz,

$$Kv(25\ \text{kHz}) = \frac{1}{Kmod\,Gv(25\ \text{kHz})} \tag{25}$$

Recalling the values of K_{mod} and G_V (25 kHz) found in Equations 22 and 23, K_V (25kHz) is determined:

$$Kv(25\ \text{kHz}) = \frac{1}{(0.422)(0.5)} = 4.74 \qquad (26)$$

4.2.6.4 Placing a zero in $K_v(s)$

Usual practice is to design the voltage loop so that it contains a zero at or below the output filter resonant frequency, to provide phase boost to compensate for the phase lag of the output filter. Thus, $K_v(s)$ should have the form:

$$Kv(s) = \frac{K(1+Ts)}{s} \qquad (27)$$

where $T = 1/(2\pi f_Z)$, and f_Z is the frequency of the zero.

Referring to the Bode plots of $G_i(s)$ (Figures 5 and 8), the resonant frequency of the output filter is approximately 2.3 kHz. In the absence of the Bode plots, this can be calculated from:

$$f = \frac{10^6}{6.28\,(1200)(3.9)} = 2.33\ \text{kHz} \qquad (28)$$

The zero of $K_v(s)$ will thus be placed at kHz by choice.

The time constant, T, in Equation 27 can now be determined:

$$T = 1/(2\pi f_Z) = 1/(6.28)(1{,}000) \qquad (29)$$
$$= 1.59 \times 10^{-4}$$

At 25 kHz, which is well above the 1 kHz zero, Equation 27 reduces to:

$$Kv(25\ \text{kHz}) = \frac{K(1+Ts)}{s} = KT \qquad (30)$$

which allows calculation of K as follows:

$$K = Kv(25\ \text{kHz})/T \qquad (31)$$
$$= 4.74/(1.59 \times 10^{-4}) = 3 \times 10^4$$

The final expression for K_v can now be written:

$$Kv(s) = \frac{3 \times 10^4 (1 + 1.59 \times 10^{-4} s)}{s} \qquad (32)$$

4.2.6.5 Calculating component values

It would appear that the circuit configuration shown in Figure 3, namely R1, R2, C1, R5, R6, R7, and R8, satisfy the requirement for high dc gain at the reference/amplifier U4, and a zero which can be set by choice of C1 and R2. However several DC operating constraints introduce some difficulties:

1. The output of the optocoupler (junction of R6 and R7) should be restricted to a fairly narrow range (perhaps ±1V) so as not to alter its operating point and transfer characteristics over the range of required converter operation.

2. The output of the error amplifier (applied to the PWM input of U2) must be able to swing over the full range of the ramp, to provide full control of the converter.

3. The DC operating point of U4 must remain fairly well centered for proper, linear operation. It should not be required to saturate or approach cutoff.

The above constraints lead to practical choices for R5, R6, and R7 as follows:

R5. To minimize operating current requirements in the control circuit, the optocoupler will be operated at a nominal output current of 1 mA. The MOC8102 data shows that the current transfer ratio at 1 mA is approximately 1.0 and therefore the input (LED) current will also be 1 mA. Further, the LED forward voltage drop is typically 1.05 V, but may be as high as 1.5 V due to production variations and temperature. The output of U4 must be kept well above the input reference voltage of 2.5 V.

The choice of 390 ohms for R5 is consistent with these requirements. Nominally the cathode of U4 will be at 5 –1.15 –(1)(0.39) = 3.46 V. If the LED voltage is 1.5 V, the cathode of U4 will be 3.11 V, and U4 will still operate properly. Additional allowance must be made for the variation in LED current as the operating point of the converter changes. This will be determined by the choices of R6, R7, and R8.

$$R5 = 390\ \Omega \tag{33}$$

R6. Assuming that the values of R7 and R8 will be chosen for enough gain to keep the optocoupler current fairly constant (perhaps within 0.3 mA of the 1 mA center value), R6 is the main determinant of the nominal optocoupler current. The reference voltage of U2 is 2.5 V, and this is the voltage which will appear at the junction of R7 and R8. Setting the nominal voltage at the emitter of the optocoupler (the high side of R6), leads to the choice of R6:

$$R6 = \frac{2.5\ \text{V}}{1\ \text{mA}} = 2.5\ \text{k}\Omega \quad \textit{Use}\ 2.7\ \text{k}\Omega \tag{34}$$

R7. The choice of R7 is not tightly bounded. It should be high enough so that the current in the optocoupler remains fairly constant over the control range, and be low enough to maintain low impedance at the amplifier to avoid unnecessary noise pickup. A reasonable choice is 10 k ohms.

$$R7 = 10\ \text{k}\Omega \tag{35}$$

C1. The overall transfer function of U4, U1 (optocoupler), and the error amplifier in U2, is really K_V. To visualize this signal path, Figure 9 is extracted from Figure 3.

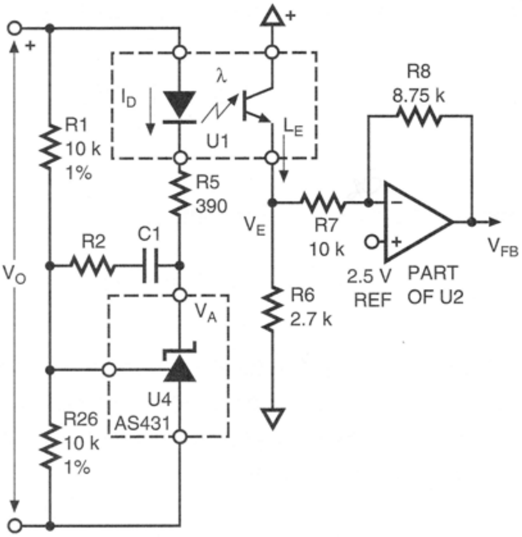


Figure 9. Voltage Feedback, Version 1

Inspection of Figure 9 shows that:

$$Kv = \frac{V1b}{Vo} = \frac{Va}{Vo}\,\frac{Id}{Va}\,\frac{Ie}{Id}\,\frac{Ve}{Ie}\,\frac{R8}{R7} \tag{36}$$

The terms of this expression are as follows:

$$\frac{Va}{Vo} = -\frac{1 + sC1R2}{sC1R1} \tag{37}$$

$$\frac{Id}{Va} = \frac{1}{Va}\,\frac{Vo - Va}{R5} = \frac{1}{R5}\left(\frac{Vo}{Va} - 1\right)$$

$$\frac{Id}{Va} = \frac{1}{R5}\left(-\frac{sC1R1}{1 + sC1R2} - 1\right)$$

$$\frac{Id}{Va} = -\frac{1}{R5}\left(\frac{1 + sC1(R1 + R2)}{1 + sC1R2}\right) \tag{38}$$

$$\frac{Ie}{Id} = \textit{Current Transfer Ratio (CTR)} = 1 \tag{39}$$

$$\frac{Ve}{Ie} = \frac{R6\,R7}{R6 + R7} \tag{40}$$

The complete expression for K_V is therefore:

$$Kv(s) = \frac{1}{R1R5C1}\left(\frac{1 + sC1(R1 + R2)}{s}\right)\frac{R6R8}{R6 + R7} \qquad (41)$$

which is of the form of Equation 32:

$$Kv(s) = \frac{3\times10^4(1+1.59\times10^{-4}s)}{s} \qquad (32)$$

These two expressions for $K_v(s)$ can be equated to derive the values of the unknown components, R2, R8 and C1. First, lets be large and neglect the “1” in the numerator. The result is:

$$\frac{(R1 + R2)R6R8}{R1R5(R6 + R7)} = \frac{3\times10^{4}\ (1.59\times10^{-4})}{1} \qquad (42)$$

The concern at this point is that, due to the minimum gain limitation at U4 which was explained in Section 4.2.6(3), it may be difficult to meet the requirement imposed by Equation 42. It is clear from inspection that R2 should be minimized, since it appears in the numerator only. Setting it to 0 and solving for the only remaining unknown yields the following:

$$R8 = 8.75\ \mathrm{k}\Omega \qquad (43)$$

Although this value will produce the required dynamics, it is intolerable. The reason is that it reduces the gain of the U2 error amplifier to such a low value that the output of the opto-coupler cannot provide a big enough swing to cause the error amplifier's output to cover the ramp, whose amplitude (V_{ramp}) is 2.368 V, as found in Equation 21.

4.2.6.6 An improvement

The solution to this dilemma is to raise R8 to a value which will provide this necessary voltage

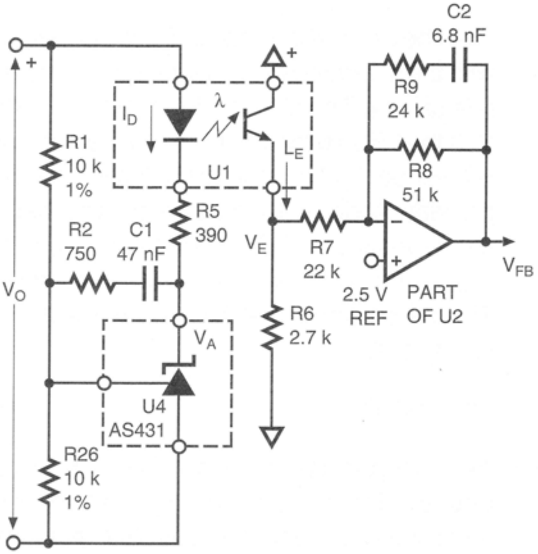


Figure 10. Voltage Feedback, Version 2

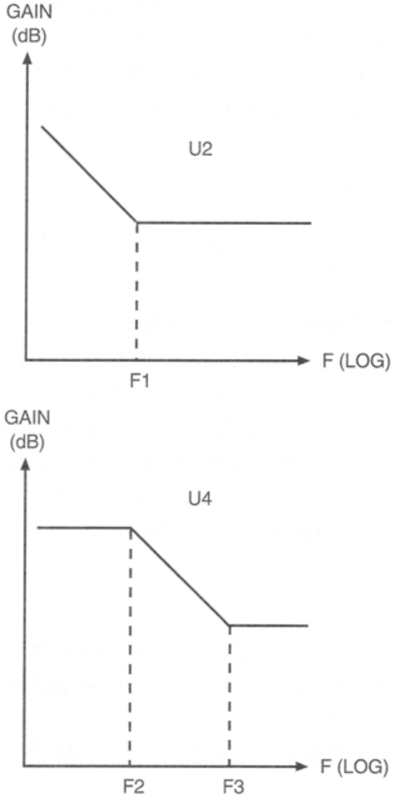


Figure 11. Frequency Response of U2 and U4

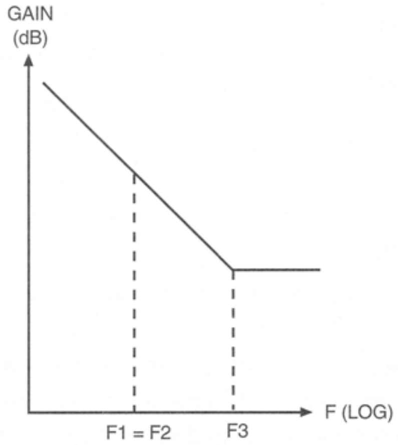


Figure 12. Combined Response with $f1 = f2$

range, and then add a resistor-capacitor branch (R9 and C2) across R8 to reduce its gain at high frequency. This results in the circuit configuration shown in Figure 10. Examining the two amplifiers, U2 and U4, results in the Bode plots of Figure 11. If the zero of U4 is set equal to the pole of U2, the overall response will have only a single zero, as shown in Figure 12.

The expression for the response of the new circuit is still of the form of Equation 36. Before allowing the U4 zero to cancel the U2 pole, the expression for K_v is:

$$Kv(s) = \frac{1}{R1R5C1}\left(\frac{1 + sC1(R1 + R2)}{s}\right) \times \frac{R6R7}{R6 + R7}\frac{R8}{R7}\frac{(1 + R9C2s)}{(1 + (R8 + R9)C2s)} \quad (44)$$

Setting the zero of U4 equal to the pole of U2 simplifies the expression, since it implies that:

$$C1(R1 + R2) = C2(R8 + R9) \quad (45)$$

and the simplified expression for $K_v(s)$ is:

$$Kv(s) = \frac{1}{R1R5C1}\frac{R6R8(1 + R9C2s)}{s(R6 + R7)} \quad (46)$$

Comparing this to the form of $K_v(s)$ given in Equation 32:

$$Kv(s) = \frac{3 \times 10^4(1 + 1.59 \times 10^{-4}s)}{s} \quad (32)$$

suggests the coefficients be set equal, hence:

$$\frac{R6R8}{R1R5C1(R6 + R7)} = 3 \times 10^4 \quad (47)$$

and

$$R9C2 = 1.159 \times 10^4 \quad (48)$$

All are known except C1 and R8. Rearranging terms yields:

$$\frac{R8}{C1} = 3 \times 10^4 \frac{R1R5(R6 + R7)}{R6} \quad (49)$$

Before substituting values into this equation, a decision is made to raise the value of R7 from 10 k to 22 k ohms, to require less sink current capability of the amplifier in U2.

$$R7 = 22\ \text{k}\Omega \quad (50)$$

Substituting the known values gives:

$$R8 = C1(3 \times 10^4)(10^4)(390)(22,000 + 2,700)/2,700 \quad (51)$$
$$= C1(1.07 \times 10^{12})$$

A desirable value for R8 would be in the neighborhood of 50 k to 100 k ohms. If 50 k is chosen, the value of C1 will be 50,000/1.07 × 1012, or 0.0467 µF. Let C1 be 47 nF, and solve for R8. R8 = 50.2 k ohms. Use 51 k ohms.

$$C1 = 47\ \text{nF} \quad (52)$$

and

$$R8 = 51\ \text{k}\Omega \qquad (53)$$

It is now left to determine the values of C2, R2, and R9. Equations 32 and 46 demand that:

$$R9C2 = 1.59 \times 10^{-4} \qquad (54)$$

Further, Equation 45 states that:

$$C1(R1 + R2) = C2(R8 + R9) \qquad (45)$$

It appears that R2 could be set equal to zero. If this is done, then Equation 45 simplifies to:

$$C1R1 = C2(R8 + R9) = C2R8 + C2R9 \qquad (55)$$

Note that C1, R1, R8 and C2 × R9 are known, so C2 can be found:

$$C2 = \frac{C1R1 - C2R9}{R8} \qquad (56)$$

$$C2 = \frac{(0.047 \times 10^{-6})(10^{4}) - 1.59 \times 10^{-4}}{51{,}000} \qquad (57)$$

This yields C2 = 0.0061 µF. If the next larger standard value of C2 is chosen, a corresponding value for R2 can be found:

$$Use\ C2 = 6.8\ \text{nF} \qquad (58)$$

$$R2 = \frac{C2R8 + C2R9 - C1R1}{C1} \qquad (59)$$

$$R2 = \frac{(3.47 \times 10^{-4}) + (1.59 \times 10^{-4}) - (0.047 \times 10^{-6})10^{4}}{0.046 \times 10^{-6}}$$

$$R2 = 766\ \Omega$$

$$Use\ R2 = 750\ \Omega \qquad (60)$$

Now use Equation 54 to solve for R9:

$$R9C2 = 1.59 \times 10^{-4} \qquad (54)$$

$$Use\ R9 = 24\ \text{k}\Omega \qquad (61)$$

4.3 Results

Figure 13 shows the closed loop response of the converter. Unity gain crossover occurs at 50 kHz as expected, and the phase margin is approximately 86 degrees. Figure 14 is an oscilloscope photo showing the output voltage response for a 5 A to 10 A load change. The obvious first-order recovery waveshape is consistent with the high phase margin.

The recovery time of approximately 0.4 ms is consistent with the 1 kHz zero of the voltage loop response, and can be made better if the zero is moved up in frequency.

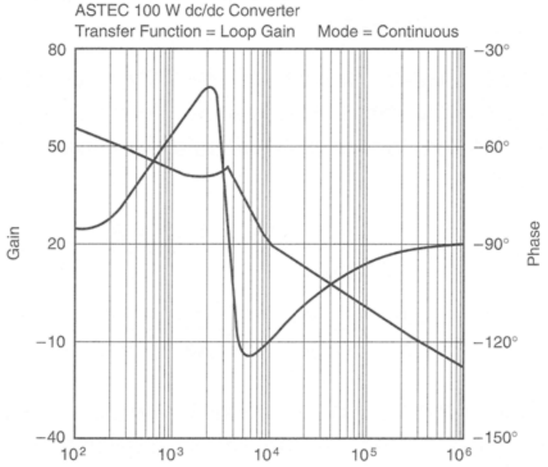
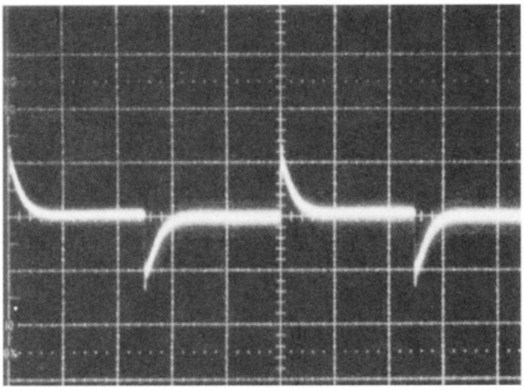
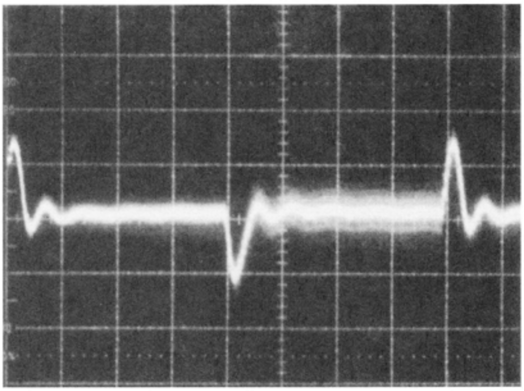


Figure 13. Closed Loop Response



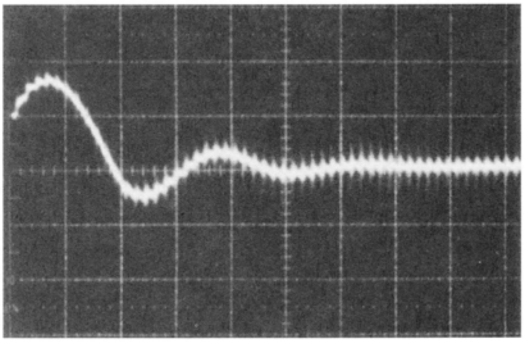
Vo, with 5 A to 10 A Load Change
0.1 V × 1 ms/div.

Figure 14. Transient Response



Vo, with 4 A to 8 A Load Change
0.1 V × 50 µs/div.

Figure 15. Improved Transient Response



Vo, with 4 A to 8 A Load Change
0.1 V ¥ 10 ms/div.

Figure 16. Same as Figure 15., but at 10 ms/div.

4.4 Faster Transient Response

Moving the voltage loop's zero from 1 kHz to 10 kHz results in much faster transient response, as shown in Figures 15 and 16. The component values for this modification are:

C1 = 4.7 nF

C2 = 1 nF

R2 = 4.3 kΩ

R9 = 16 kW

There is a price to pay for this speed, however, and it is the gain margin, as shown in the Bode plot of Figure 17.

For an unconditionally stable system the gain should be less than unity whenever the phase lag exceeds 180 degrees. Although the converter is obviously stable in the waveform photograph of Figure 15, it may be unstable at low input or lightload. Further work in the area of phase boost in the voltage feedback might allow satisfactory operation with this higher frequency zero placement; a proper challenge for the ambitious designer!

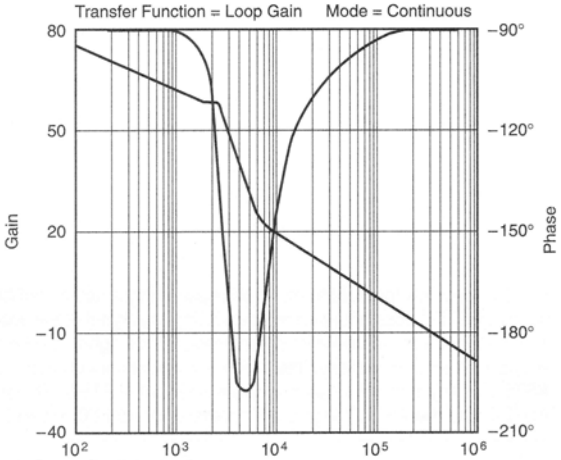


Figure 17. Loop Response with Zero of Voltage Loop at 10 kHz

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AS3842
Application Note 6

SWITCHING POWER SUPPLY CONTROL LOOP DESIGN

1. Introduction

In a switched mode power converter, the conduction time of the power switch is regulated according to the input and output voltages. Thus, a power converter is a self-contained control system in which the conduction time is modulated in reaction to changes in the input and output voltages. From a theoretical approach, control loop design often involves complicated equations, making control a challenging but often misunderstood area in switched mode power supply design. A simplified approach to feedback control loop analysis is presented in the following pages, beginning with a general overview of various parameters affecting performance in a switching power system. A demonstration of an actual power supply is given to show the components involved in designing the characteristics of the control loop. Test results and measurement techniques are also included.

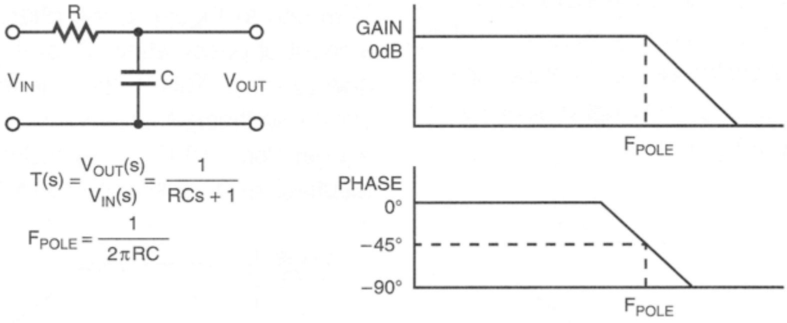
2. Basic Control Loop Concepts

2.1 Transfer Functions and the Bode Plots

The transfer function of a system is defined as the output divided by the input. It consists of a gain and a phase element that can be plotted separately in a Bode plot. The gain around a closed loop system is the product of the gains of all the elements around the loop. In a Bode plot, the gain is plotted logarithmically. Since the product of two numbers is their logarithmic sum, their gains can be summed graphically. The phase of the system is the sum of all phase shifts around the loop.

2.2 Poles

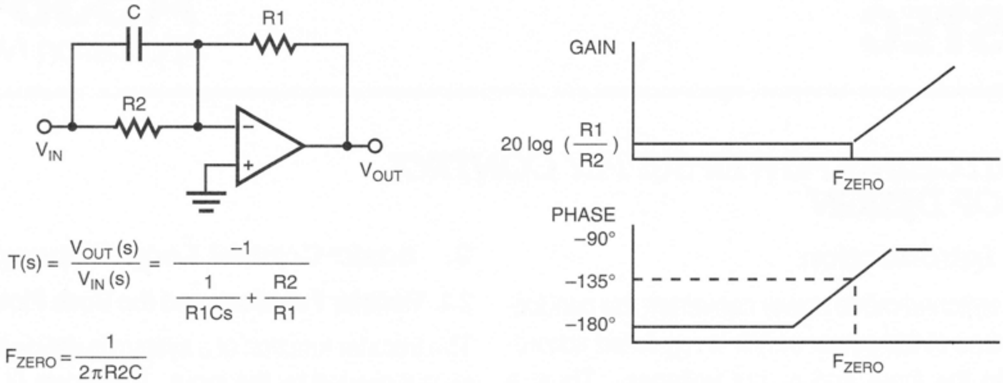
Mathematically, in a transfer equation, a pole occurs when its denominator becomes zero. Graphically, a pole in the bode plot occurs when the slope of the gain decreases by 20 dB per decade. Figure 1 illustrates a low pass filter commonly used for creating a pole in the system. Its transfer function and Bode plots are also shown.



$$T(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{1}{RCs + 1}$$

$$F_{POLE} = \frac{1}{2\pi RC}$$

Figure 1.



$$T(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{-1}{\frac{1}{R1Cs} + \frac{R2}{R1}}$$

$$F_{ZERO} = \frac{1}{2\pi R2C}$$

Figure 2.

2.3 Zeros

A zero in frequency domain transfer function occurs when the numerator of the equation goes to zero. In a Bode plot, a zero occurs at a point where the slope of the gain increases by 20 dB per decade accompanied by 90° phase lead. A high pass filter circuit causing a zero is depicted in figure 2.

There is a second type of zero, known as a right half plane zero, that causes phase lag instead of phase lead. A right half plane zero causes a 90° phase lag, accompanied by an increase in gain. Right half plane zeros are usually found in boost and buck-boost converters and so extra precaution should be taken during feedback compensation design so the crossover frequency of the system is well below the frequency of the right half plane zero. The Bode plot of a right half plane zero is shown below in figure 3.

3.0 Ideal Gain-phase Plots for a Switching Mode Power Supply

A goal must be clearly defined prior to designing any control system. Generally, the goal is simply a Bode plot constructed to achieve the best system dynamic response, tightest line and load regulation, and greatest stability. An ideal closed loop Bode plot should possess three characteristics: sufficient phase margin, wide bandwidth, and high gain. A High phase margin damps oscillations and shortens the transient settling time. Wide bandwidth allows the power system to quickly respond to sudden line and load changes. A High gain ensures good line and load regulation.

3.1 Phase Margin

Referring to Figure 4, the phase margin is the amount of phase above 0° at the crossover frequency (fcs). This is different from most control system textbooks that present a measuring phase margin from -180°. They include the negative feedback at DC that gives them 180° phase shift

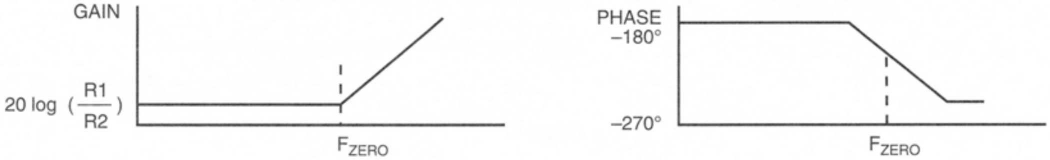


Figure 3.

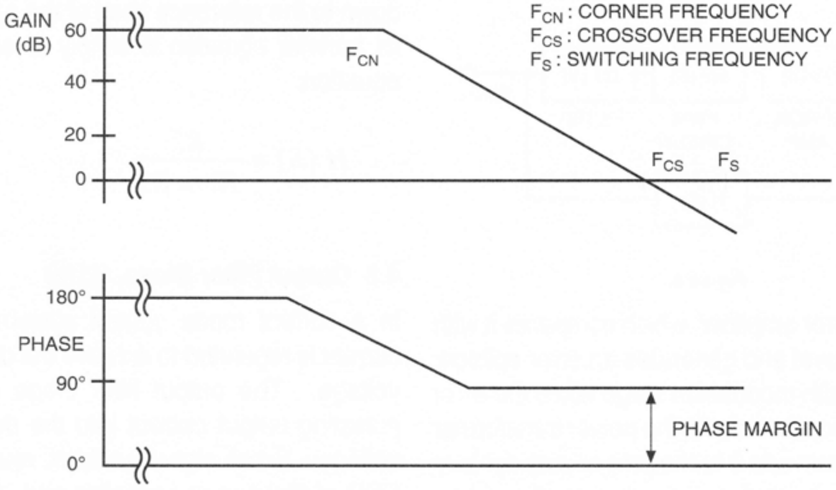


Figure 4.

at the beginning. In the actual measurement, the 180° phase shift is compensated at DC and enables the phase margin to be measured from 0°.

According to Nyquist's stability criterion, a system is stable when its phase margin exceeds 0°. However, a region of marginal stability exists where the system transient response oscillates and eventually damps out after a long settling time. A system is marginally stable if its phase margin is less than 45°. A phase margin above 45° provides the best dynamic response, short settling time and minimal amount of overshoot.

3.2 Gain-Bandwidth

The gain-bandwidth is the frequency at which the gain is unity. In figure 4, the gain- bandwidth is the crossover frequency, f_{CS}. A major limiting factor of the maximum crossover frequency is the power supply switching frequency. According to sampling theory, if the sampling frequency is less than 2 times the frequency of the information, the information will not be properly read.

In a switched mode power supply, the switching frequency is seen in the output ripple, which is false information and must not be transmitted by the control loop. Therefore, the crossover frequency of the system must not exceed half the switching frequency. Otherwise, the switching noise, the ripple, distorts the desired information, the output voltage, causing the system to be unstable.

3.3 Gain

High system gain contributes significantly to ensuring good line and load regulation. It enables the PWM comparator to accurately change the power switch duty cycle in response to variants in the input and output voltage. Often, a tradeoff needs to be determined between higher gain and lower phase margin.

4. A Practical Design Analysis Example

Applying classical control loop analysis techniques, the control loop of a switching regulator is divided into four main stages, output filter, PWM circuit, error amplifier compensation, and feedback . Figure 5 illustrates a block diagram of the four stages and figure 6 illustrates a power supply circuit diagram.

The output voltage is first divided down by the feedback network. The feedback voltage is then

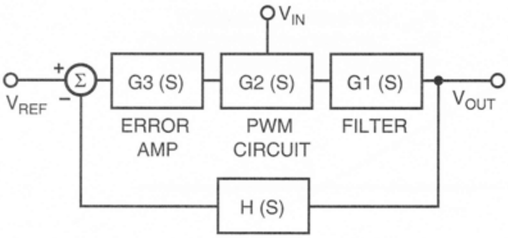


Figure 5.

fed into an error amplifier, which compares it with a reference level and generates an error voltage. The pulse width modulation stage takes the error voltage and compares with the power transformer current and converts it to the proper duty cycle to control the amount of power pulsing to the output stage. The output filter stage smoothes out the chopped voltage or current from the power transformer, completing the feedback control loop. The following determines gain and phase of each stage and combines them to form the system transfer function and the system gain and phase plot.s.

4.1 Feedback Network, H(s):

The feedback network divides the output voltage down to the reference level of the error amplifier. Its transfer equation is simply a resistor divider equation:

$$H(S) = \frac{R2}{R1 + R2} \tag{1}$$

4.2 Output Filter Stage, G1(s)

In a current mode control system, the output current is regulated to achieve the desired output voltage. The output filter stage converts the pulsating output current into the desired output voltage. Small signal analysis reveals that the ESR of the output capacitor and the feedback network resistors ($R_1 + R_2 = R_{FB}$) dictate the

$$R_{FB} = R1 + R2 \tag{2}$$

$$V_{OUT(S)} = I_{OUT(S)} \left[R_{FB} \parallel \left(\frac{1}{CS} + ESR \right) \right] \tag{3}$$

$$G1(S) = \frac{V_{OUT(S)}}{I_{OUT(S)}} = \frac{R_{FB}\,(1 + ESRCS)}{(R_{FB} + ESR)\,CS + 1} \tag{4}$$

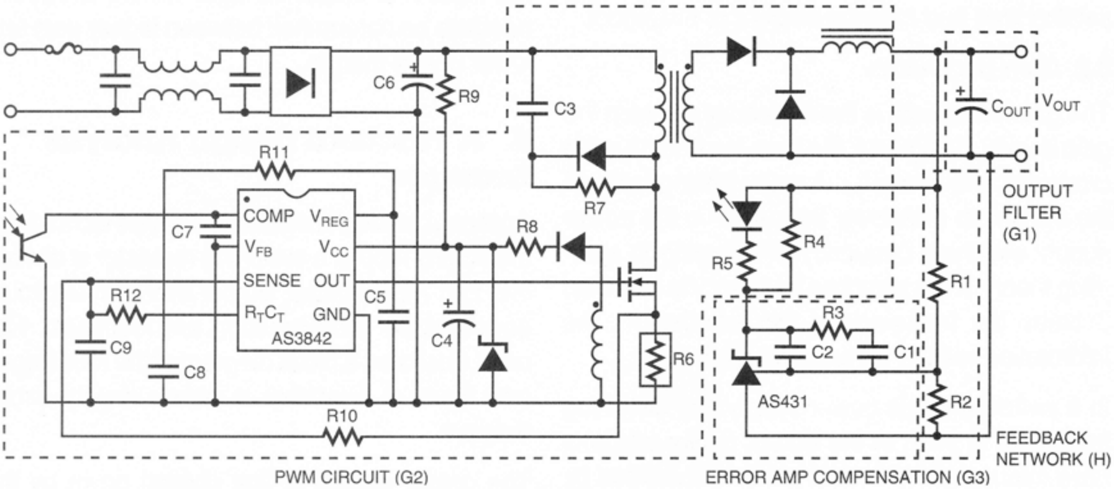


Figure 6.

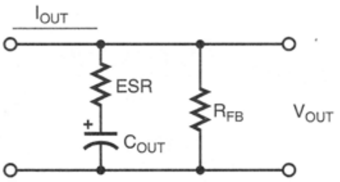


Figure 7.

characteristics of the output filter transfer function. The circuit analysis in Figure 7 demonstrates the effects of ESR and Rsense.

Transfer equation G1(s) shows an initial low frequency gain of Rsense. The gain starts to roll off at fpole = 1/2π(Rsense+ESR)C and levels off at fzero = 1/2πESRC. The Bode plots of G1(s) are shown in figure 8.

4.3 PWM Circuit Stage, G2(s)

The optocoupler circuit transfers the error signal created by the error amplifier network to the primary side. The AS3842 PWM circuit compares the error voltage with current through primary side of the power transformer. The duty cycle of the power FET is then modulated to supply sufficient current to the secondary to maintain a desired output level.

The small signal transfer function of the optocoupler has a constant gain proportional to the current transfer ratio of the optocoupler, R6 a current limit resistor in series with the optocoupler diode, and the output impedance of the AS3842 error amplifier. This is discussed extensively in the application note "Secondary Error Amplifier with the AS431." The transfer function from the output of the error amplifier to the comp pin of the AS3842 is:

$$\frac{\Delta V_{COMP}}{\Delta V_{CATHODE}} = \frac{CTR}{\underset{R5}{R6}} R_{COMP} \qquad (5)$$

Vcathode is the cathode voltage of the AS431 and the output of the compensation error amplifier. CTR is the current transfer ratio of the optocoupler. R6 is the current limit resistor in series with the optocoupler diode. Rcomp is the output impedance of the AS3842 Comp pin when it tries to source above its maximum output current.

After the error signal is transferred to the compensation pin, it is compared with a current sense signal. Figure 9 shows a simplified block diagram of the current sense comparator and switching stages.

In a closed loop system Vcomp is maintained in the same level as Isense; therefore, Iprimary is effectively regulated by Vcomp.

$$I_{PRIMARY} = \frac{V_{COMP}}{R_{SENSE}} \qquad (6)$$

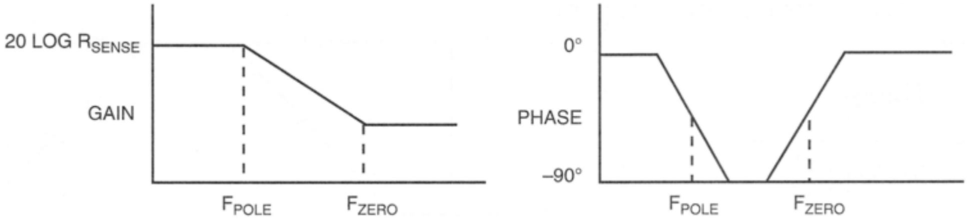


Figure 8.

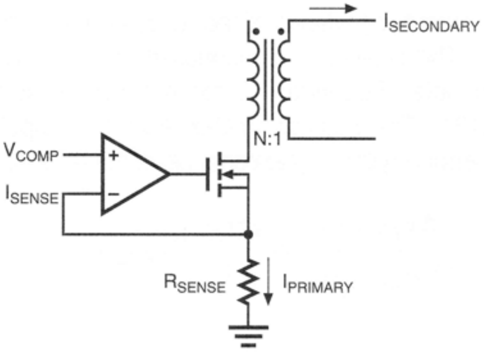


Figure 9.

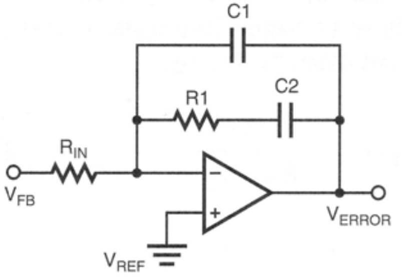
Since Isecondary, the secondary current or output current, is proportional to the primary current, equation (4) can be rearranged to show a relationship between secondary current and Vcomp.

$$\begin{aligned} I_{PRIMARY} &= \frac{I_{SECONDARY}}{N} \\ &= \frac{V_{COMP}}{R_{SENSE}} \\ &= \frac{I_{OUT}}{N} \end{aligned} \qquad (7)$$

$$\frac{\Delta V_{COMP}}{\Delta I_{OUT}} = \frac{R_{SENSE}}{N} \qquad (8)$$

The transfer function of PWM stage can be created by combining equation (3) and (6):

$$\begin{aligned} G2\,(S) &= \frac{\Delta I_{OUT}}{\Delta V_{CATHODE}} \\ &= \frac{N}{R_{SENSE}} \, \frac{CTR}{R6} \, R_{COMP} \end{aligned} \qquad (9)$$



$$G3(s) = \frac{V_{ERROR}}{V_{FB}} = \frac{1 + SR1C2}{SR_{IN}\,(C2 + C1) + SR1\,(C2 \parallel C1)}$$

$f_{p1} = 0$

$$f_Z = \frac{1}{2\pi R1C2}$$

$$f_p2 = \frac{1}{2\pi R1C2\,(\frac{C1}{C1 + C2})}$$

A = OPEN LOOP GAIN OF THE AMPLIFIER

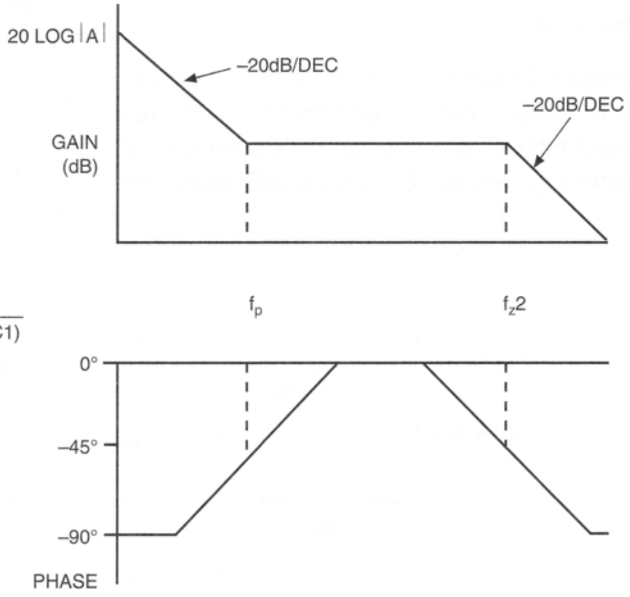


Figure 10.

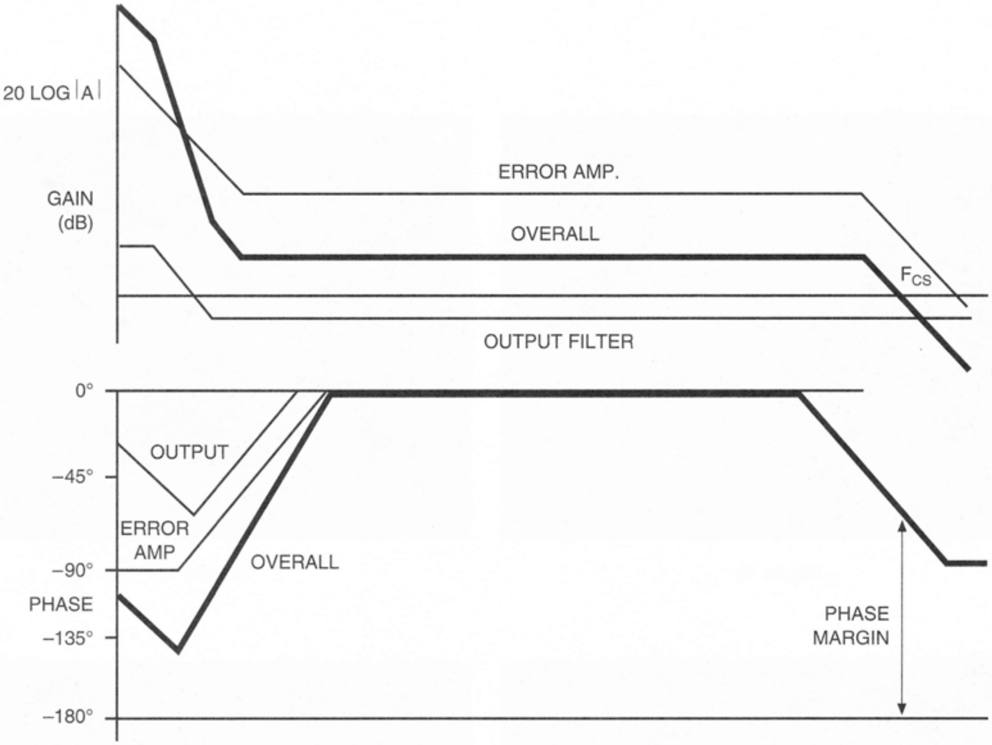


Figure 11.

Transfer function G2 consists of only gain and no phase shift.

4.4 Error Amplifier Compensation Network,G3(s)

Once the transfer functions of the output filter and PWM circuit stage are determined, the error amplifier compensation network can then be configured to achieve the optimum system performance. Figure 10 illustrates a compensation scheme that gives high frequency roll-off and high gain at low frequency.

This compensation scheme has some favorable characteristics for error amplifier compensation. It has very high DC gain and well-controlled roll off.

4.5 Overall System

Since this is a linear system, superposition technique can be applied to derive the overall system transfer function. By superimposing the gains and phases of the stages around the loop, a Bode plot of the overall system is generated. The poles and zeros of the compensation network can then be placed to optimize the system performance. Figure 11 combines the Bode plots of the stages and 180° phase shift is also added to account for the negative feedback of the system.

5. Measurement Results

A 150-watt current mode forward converter was constructed and its small signal loop characteristics modified to demonstrate its effects on system transient response. Figure 12 shows its gain-phase plot. As predicted by Figure 11, the same Bode plot curvature was acquired. The gain-phase shows the system has a phase margin of 86.7°, implying a stable system with a fast transient re-

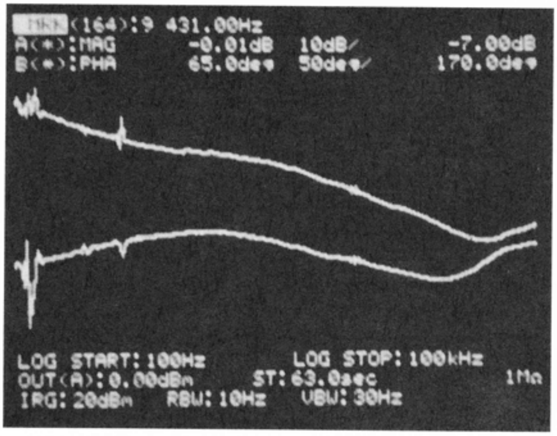


Figure 12.

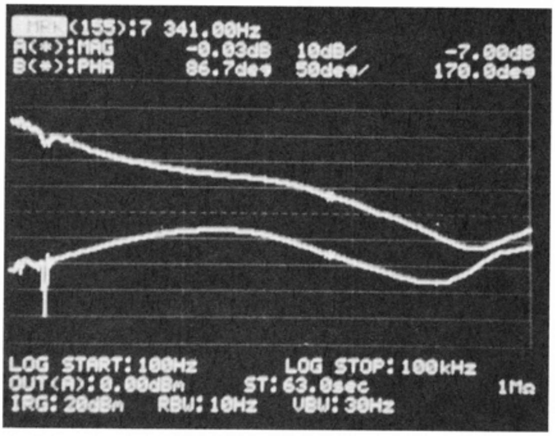


Figure 13.

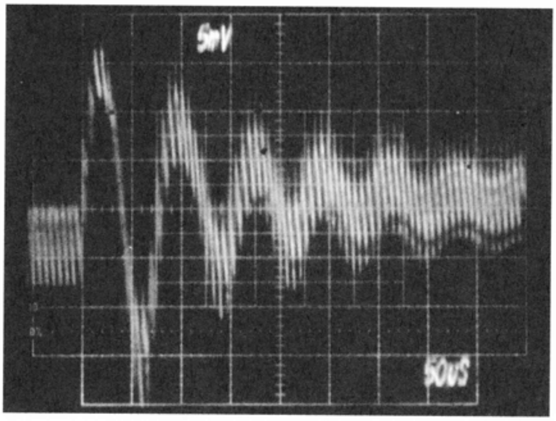


Figure 14.

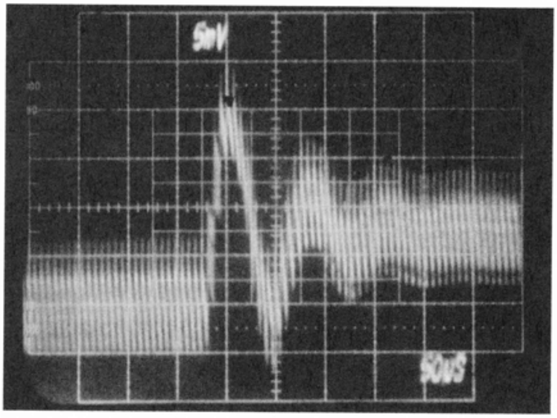


Figure 15.

sponse. Figure 13 shows the transient response of the system. To demonstrate the effects of phase margin, the phase margin of the system was decreased by increasing the overall gain of the system, increasing the crossover frequency. The phase margin decreases with increasing crossover frequency. Figure 14 shows a Bode plot of the system with higher cross over frequency and smaller phase margin of 65°. Its transient response is shown on figure 15. Note that smaller phase margin results in greater oscillation and longer settling time. Table 1 compares the changes in line and load regulations between two systems with different gain magnitudes. As discussed previously, high loop gain results in tighter line and load regulation. It should also be noted that a tradeoff has been made between the high phase margin and lower loop gain.

Load Regulation	High Loop Gain	Low Loop Gain
$V_{IN} = 85\ V_{AC}$	127 mV	132 mV
$_{IN} = 135\ V_{AC}$	101 mV	116 mV
Line Regulation		
Low Load	21 mV	25 mV
High Load	5 mV	9 mV

6.0 Measurement Techniques

To guarantee accurate results, the input impedance of the test signal injection node must be larger than its output impedance. In the test circuit (figure 6) where the error amplifier is on the secondary side and the PWM circuit is on the primary side, the test signal is injected at the output of the optocoupler and before the Vcomp input of the AS3842. The input impedance is the impedance looking into the Vcomp pin and the output impedance is the output impedance of the optocoupler. In other applications where the error amplifier can not be separated from the PWM circuitry, the test signal can be injected following the output filter capacitor, in series with the input to the error amplifier.

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Venable, D., "Practical techniques for Analyzing, Measuring and Stabilizing Feedback Control Loop in Switching Regulators and Converters," PowerCon 7 Proceedings, March, 1980, page 12. 1–12.17.

Chetty, P.R.K., "Modeling and Design of Switching Regulators," IEEE Transactions on Aerospace and Electric Systems, May 1992, page 333–343.

Jamerson, C., and Hosseini, "A Simplified Procedure for Compensation Current-Mode Control Loops," HFPC Proceedings, June 1991, page 299–318.

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Notes

Appendix

Notes

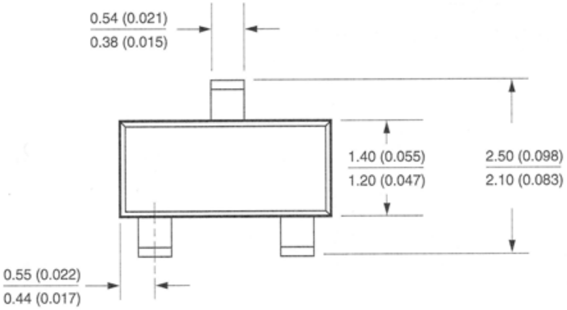
Package Outline Drawings

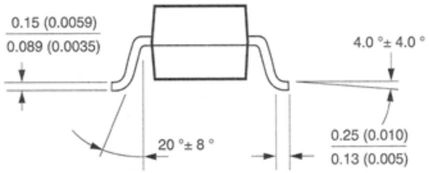
The following information applies to all packages:

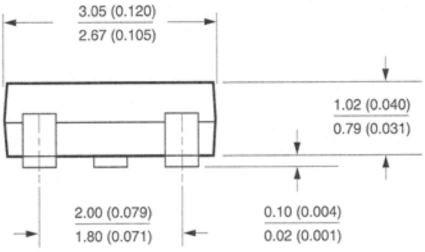
1. Dimensions are in SI units (millimeters), except for those in parentheses which are English units (inches).
2. Shoulder and lead tip dimensions are measured to the centerline of the leads.
3. Tolerances are non-cumulative.
4. Lead material is copper alloy for all packages.
5. Lead finish is solder dip or solder plate.
6. Body material is plastic (epoxy).
7. Pin 1 is denoted by a • (dot) or Δ (triangle per MIL-STD-38510H, ESDE Class 1) and will be silver or white ink, except for those packages which have a molded pin 1 depression.
8. Body dimensions do not include molding flash.

SOT-23 (VS)

Dimensions in mm (Inches)

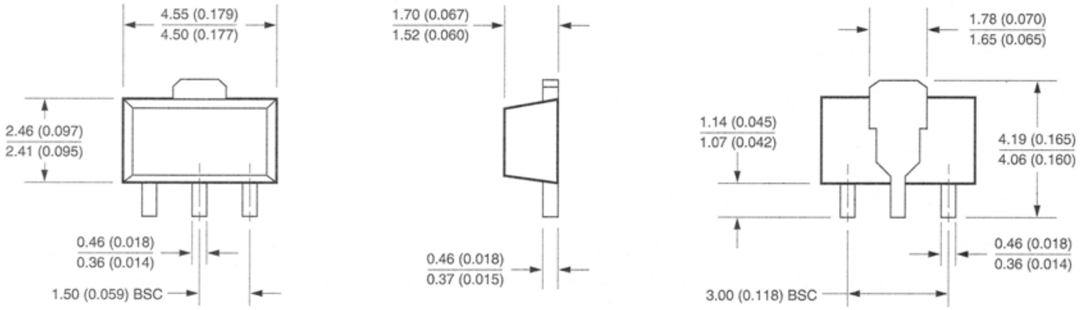






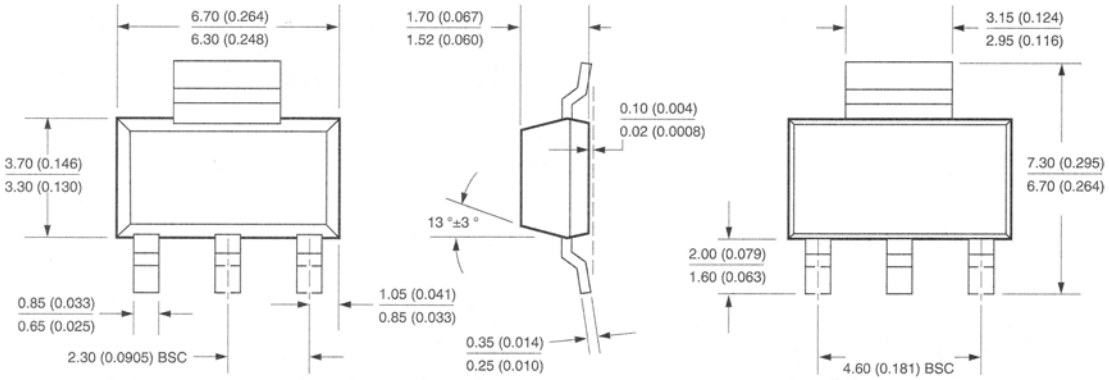
SOT-89 (S)

Dimensions in mm (Inches)



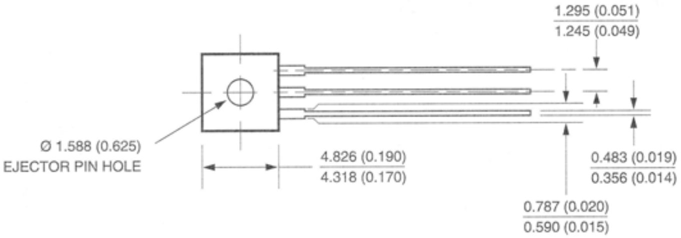
SOT-233 (G)

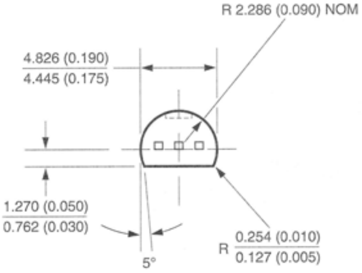
Dimensions in mm (Inches)

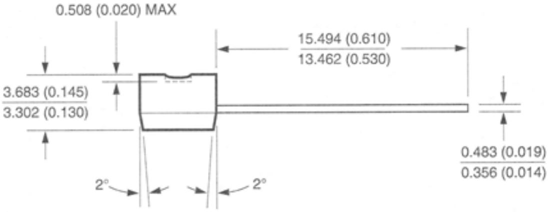


TO-92 PLASTIC (LP)

Dimensions in mm (Inches)

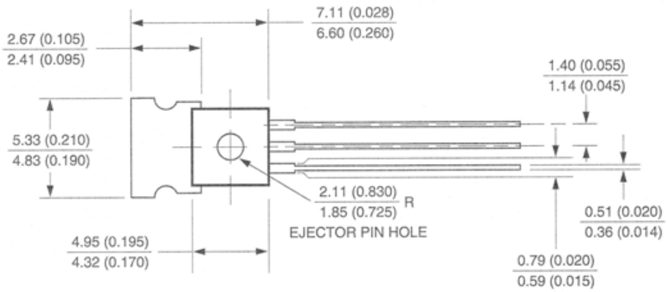


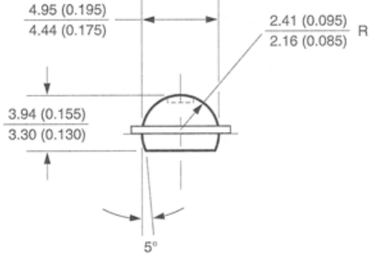


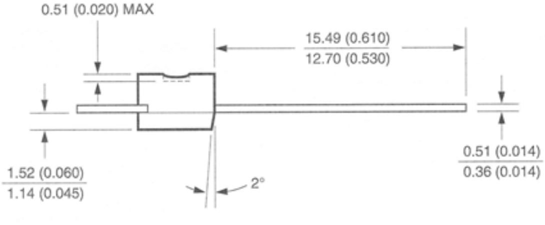


TO-237 PLASTIC (LP)

Dimensions in mm (Inches)

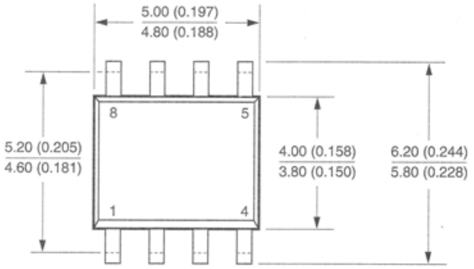


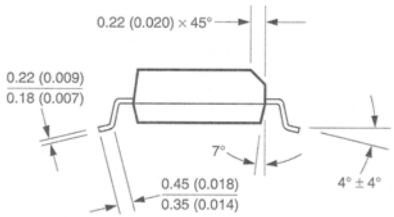


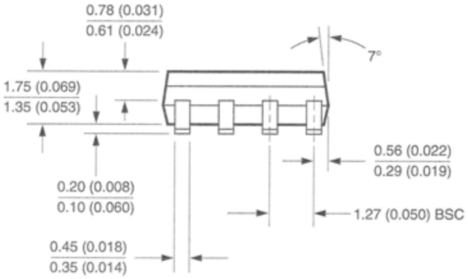


8-PIN PLASTIC SOIC (D)

Dimensions in mm (Inches)

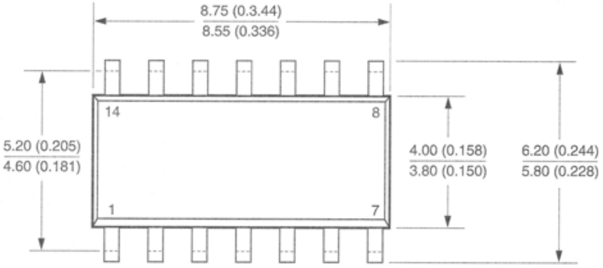


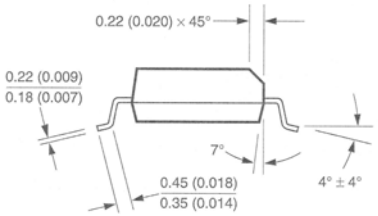


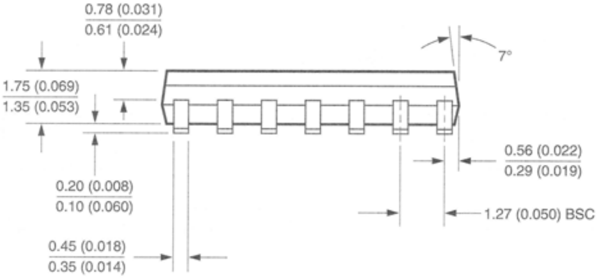


14-PIN PLASTIC SOIC (D)

Dimensions in mm (Inches)







16-PIN PLASTIC SOIC (D)

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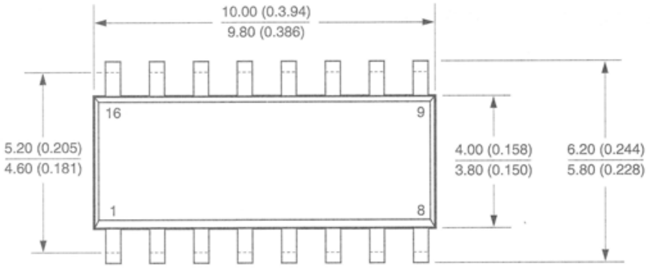
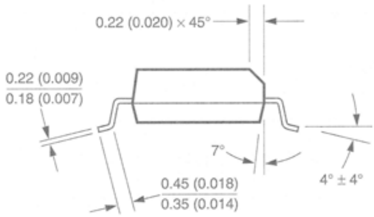
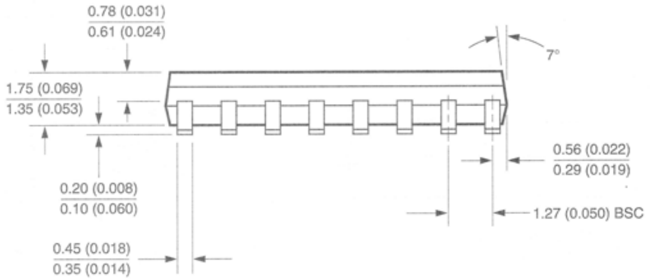
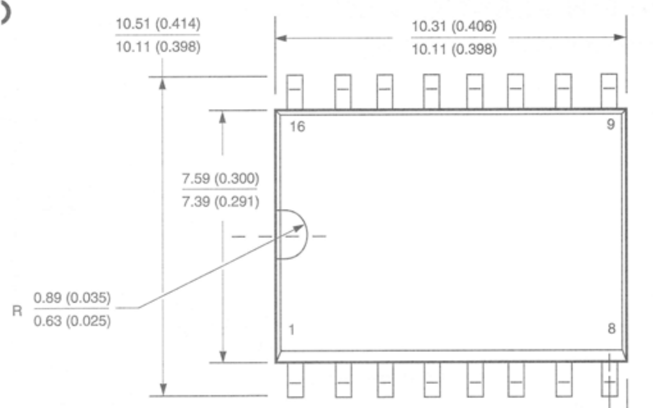


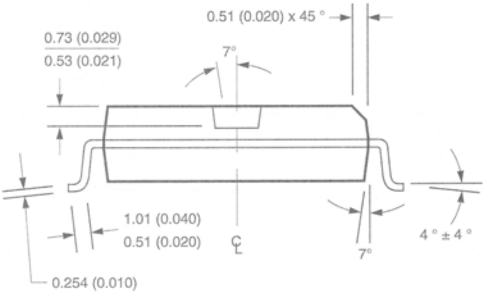


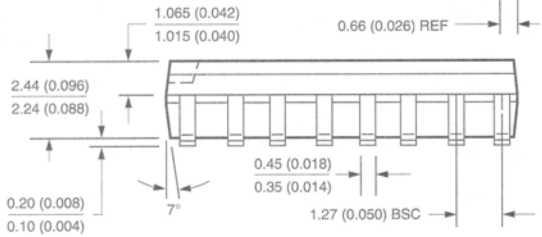


16-PIN PLASTIC SOIC-W (DW)

Dimensions in mm (Inches)

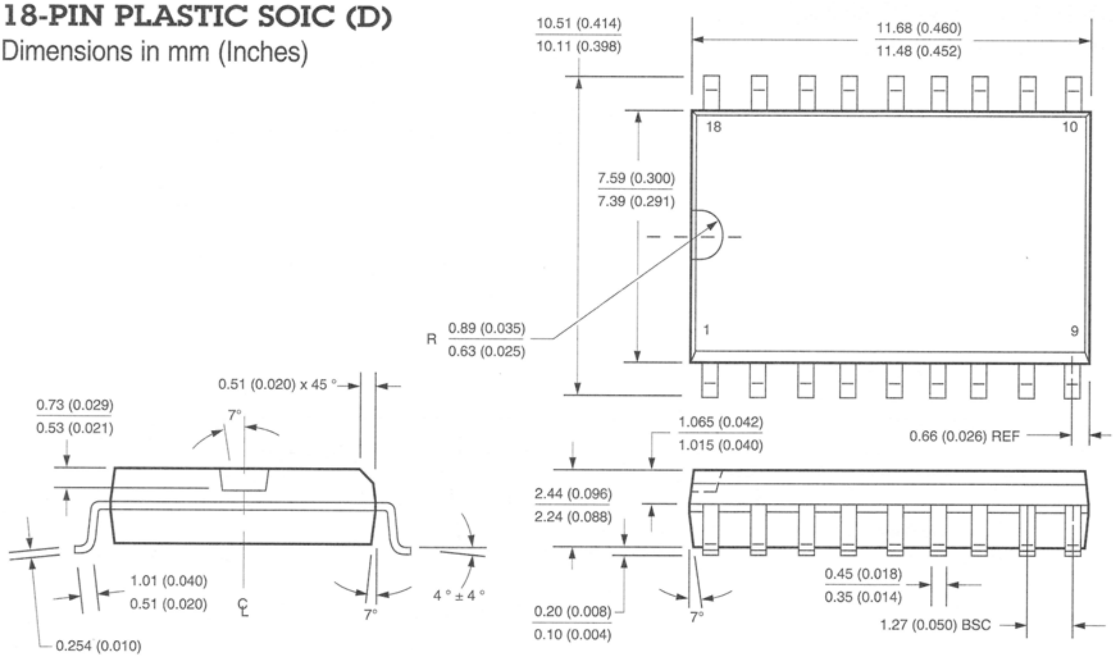






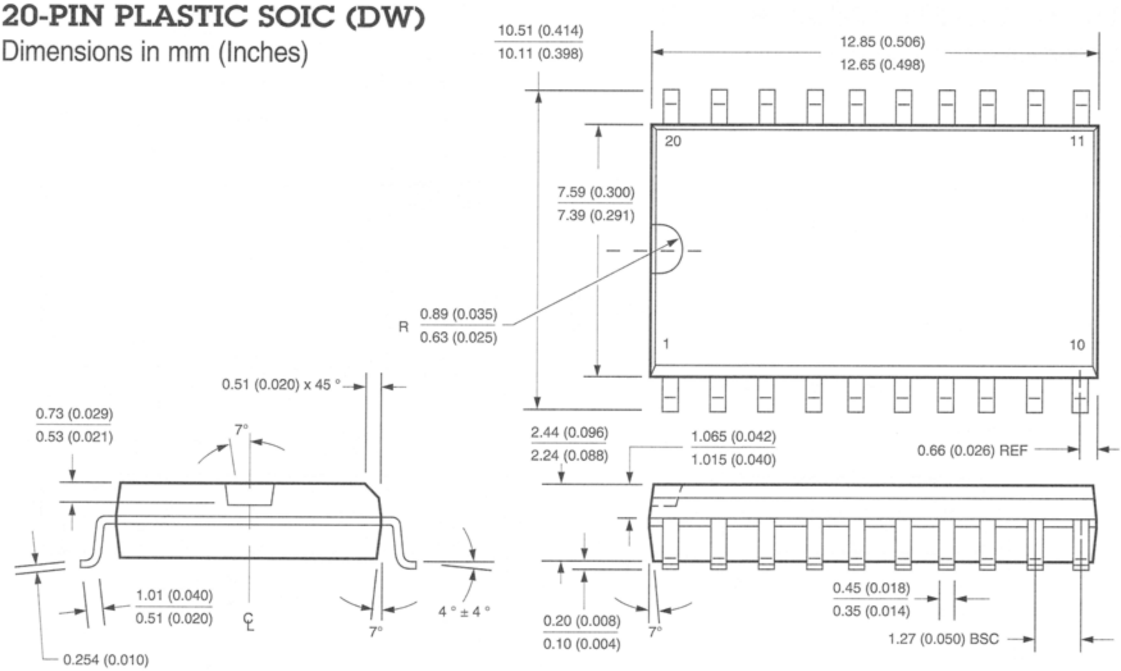
18-PIN PLASTIC SOIC (D)

Dimensions in mm (Inches)



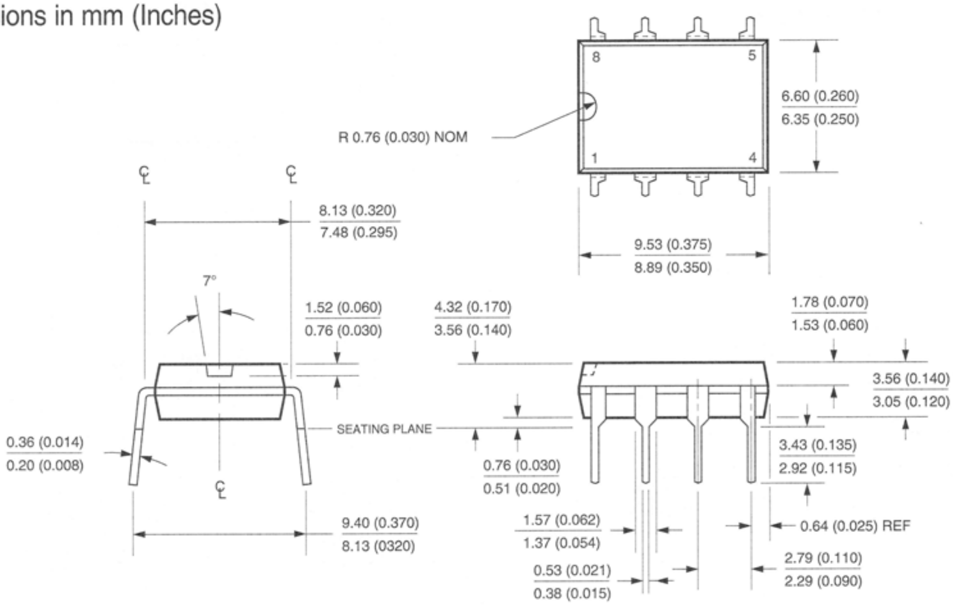
20-PIN PLASTIC SOIC (DW)

Dimensions in mm (Inches)



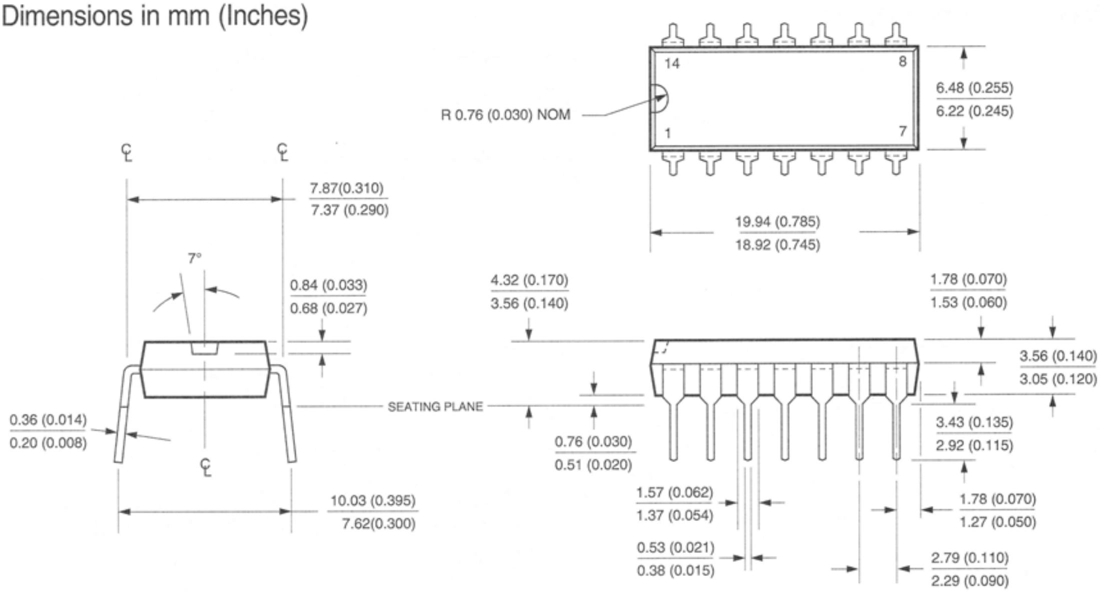
8-PIN PLASTIC DIP (N)

Dimensions in mm (Inches)



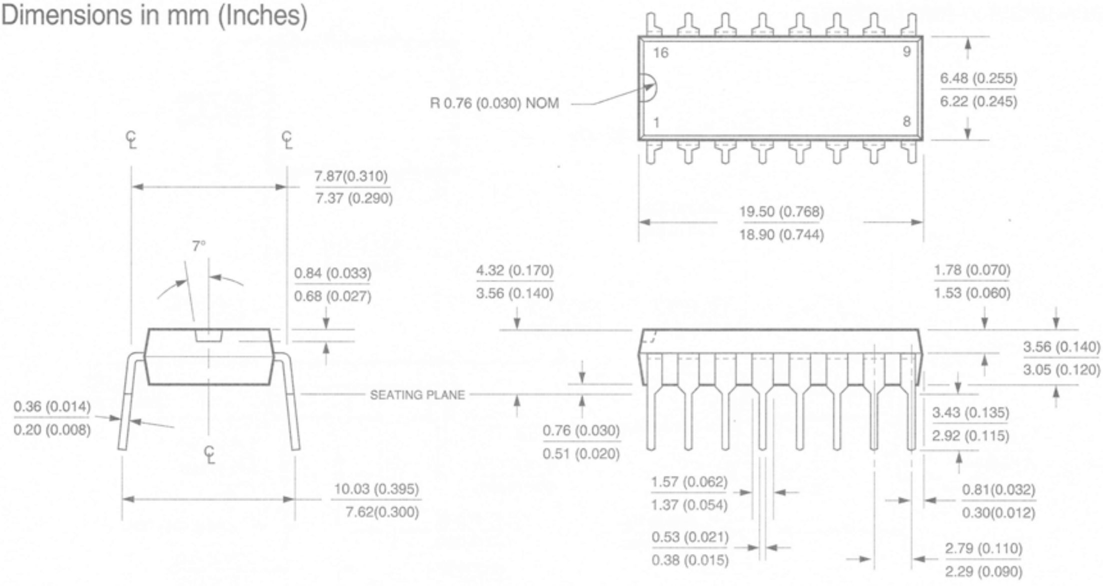
14-PIN PLASTIC DIP (N)

Dimensions in mm (Inches)



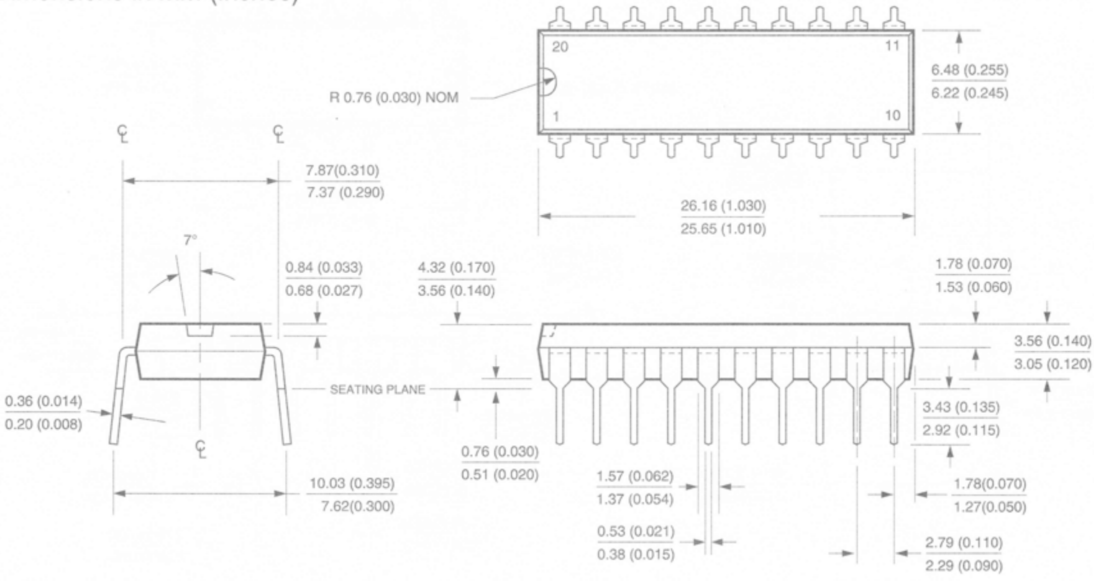
16-PIN PLASTIC DIP (N)

Dimensions in mm (Inches)



20-PIN PLASTIC DIP (N)

Dimensions in mm (Inches)



Quality Assurance and Reliability Program

Astec Semiconductor's Quality Assurance and Reliability program was developed to meet the stringent requirements for high reliability power conversion products. Being a former captive supplier to the Astec family of power supply manufacturers, Astec Semiconductor built a program that guarantees an extremely reliable product base. From tight control of layout design rules to final electrical testing of assembled parts, Astec Semiconductor strives towards continuous improvment of product reliability.

The following outline is an overview of Astec Semiconductor's quality and reliability program:

I. Lot Integrity

Wafer lot integrity maintained throughout test and assembly.

II. 100% Lot Tractability

Each part is marked with the ASTEC logo, part number, wafer lot code, assembly date code, assembly vendor, and country of origin (package size permitting)

Wafer lot travelers contain:

- test site wafer parametric data (e.g. Vbe, sheet resistivities, breakdowns)
- wafer sort data and yields by wafer
- build sheets (mini process, bond pattern, and marking specifications)
- assembly vendor travelers
- final test yields by assembly sub-lot
- final test data
- QA test results

III. ESD prevention

ESD prevention is emphasized at all levels of manufacturing and test.

IV. Wafer Lot Acceptance

Astec Semiconductor contracts wafer foundry. 5 out of 9 test sites for each wafer must pass 27 electrical specifications of our standard test pattern (incoming electrical inspection is actually comprised of well over 100 electrical tests).

Included are:

- NPN Vbe, beta, LVceo, Iceo, BVcbo, BVebo, breakdowns to substrate
- PNP Vbe, beta, LVceo, Iceo, BVcbo, breakdowns to substrate
- Sheet resistivities for base, emitter, resistor
- MOS Capacitor integrity

Wafer sort yields standardized by product and die size. Low yield wafers require engineering evaluation and disposition.

V. Device Reliability

Every assembly lot receives the following:

HTRB- High Temperature Reverse Bias to MIL-STD-883C Method 1015.7

- No/low current, operational or max voltage
- $T_a = T_j = 125°\ C$
- Sample size: 0.1% or 8 units per assembly sub-lot, whichever is greater. 96 hours minimum, 0/1 failure (One (1) failure requires engineering evaluation and material disposition).

A sample of each lot is taken for the following:

HTRB- High Temperature Reverse Bias to MIL-STD-883C Method 1015.7

- No/low current, operational or max voltage
- $T_a = T_j = 125°\ C$
- Sample size: 0.1% of production lot for 2000 hours., process monitor

OP Life-Operational Life testing:

- Operational voltage and current
- $T_j = 150°\ C$, T_a adjusted based on power dissipationof the device, low power implies 150° C ambient. 150° C temperatures not applicable to circuits with built-in over temperature shut down.
- Sample: 0.1% of production lot for 1000 hours., 0/1 failures (One (1) failure requires engineering evaluation and material disposition).

VI. Packaging Reliability

Every assembly lot receives the following:

Autoclave (Pressure Cooker) accelerated storage test:

- Unbiased
- 121° C, 14.7 psig (2 atm)
- Sample size: 0.1% or 8 units per assembly sub-lot, whichever is greater. 96 hours minimum, 0/1 failures (One (1) failure requires engineering evaluation and disposition of material.)

TO-92/TO-237 package only:

- 100% Temp Cycling to MIL-STD-883C Method 1015.7
- -65 to 150° C, 10 cycles, performed by assembly vendor

A sample of lots is taken for the following:

Autoclave (Pressure Cooker) accelerated storage test:

- Unbiased
- 121° C, 14.7 psig (2 atm)
- Sample size: 0.1% of production lot 1000 hours minimum, process monitor of vendor performance

Notes

Notes

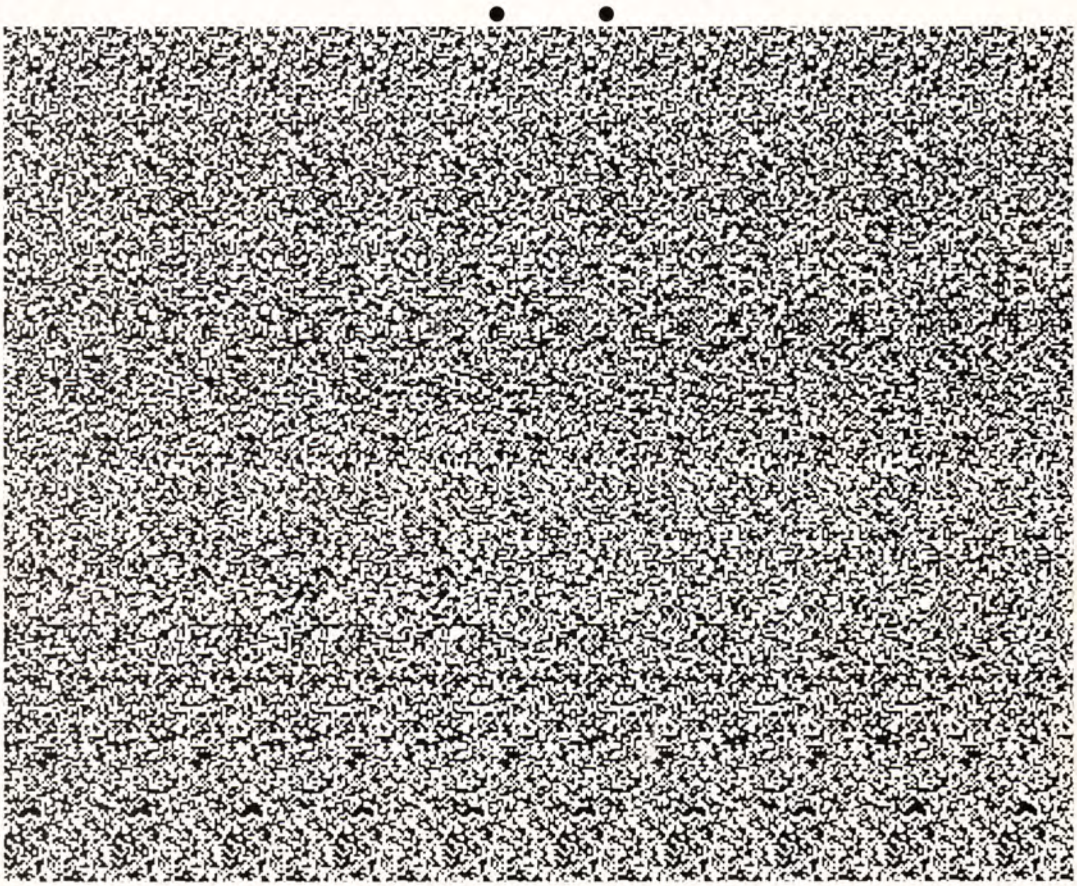
About the Back Cover ...

The back cover of the Astec Semiconductor Data Book is a three-dimensional stereogram, which can be seen by holding the image 8 to 16 inches from the face. Relax your eyes and stare straight ahead at the image.

The two dots at the top of the image will help you adjust your focus. When looking through the stereogram, you will view one set of dots with each eye. When they merge to form three dots— a strong central dot and two weak outside dots— your focus is correct.

With your focus held on the dots, look down slowly at the image. It takes the average brain anywhere from a few seconds to several minutes to translate the three-dimensional information. Have fun!

ASTEC



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